TEXAS INSTRUMENTS

ADC32RF45

SBAS747B – MAY 2016 – REVISED JULY 2016

ADC32RF45 Dual-Channel, 14-Bit, 3.0-GSPS, Analog-to-Digital Converter

1 Features

- 14-Bit, Dual-Channel, 3.0-GSPS ADC
- Noise Floor: –155 dBFS/Hz
- RF Input Supports Up to 4.0 GHz
- Aperture Jitter: 70 f_S
- Channel Isolation: 95 dB at f_{IN} = 1.8 GHz
- Spectral Performance (f_{IN} = 900 MHz):
  - SNR: 60.6 dBFS
  - SFDR: 64-dBc HD2, HD3
  - SFDR: 72-dBc Worst Spur
- Spectral Performance (f_{IN} = 1.78 GHz):
  - SNR: 58.0 dBFS
  - SFDR: 63-dBc HD2, HD3
  - SFDR: 77-dBc Worst Spur
- On-Chip Digital Down-Converters:
  - Up to 4 DDCs (Dual-Band Mode)
  - Up to 3 Independent NCOs per DDC
- On-Chip Input Clamp for Overvoltage Protection
- Programmable On-Chip Power Detectors with Alarm Pins for AGC Support
- On-Chip Dither
- On-Chip, 50-Ω Input Termination
- Input Full-Scale: 1.35 V_{PP}
- Support for Multi-Chip Synchronization
- JESD204B Interface:
  - Subclass 1-Based Deterministic Latency
  - 4 Lanes Per ADC at 12.3 Gbps
- Power Supply:
  - 1.9 V (Analog), 1.15 V (Analog), 1.15 V (Digital)
- Power Dissipation: 3.2 W/Ch at 3.0 GSPS
- 72-Pin VQFN Package (10 mm × 10 mm)

2 Applications

- Multi-Band, Multi-Mode 2G, 3G, 4G Cellular Receivers
- Phased Array Radars
- Electronic Warfare
- Cable Infrastructure
- Broadband Wireless
- High-Speed Digitizers
- Software-Defined Radios
- Communications Test Equipment
- Microwave and Millimeter Wave Receivers

3 Description

The ADC32RF45 device is a 14-bit, 3.0-GSPS, dual-channel, analog-to-digital converter (ADC) that supports RF sampling with input frequencies up to 4 GHz and beyond. Designed for high signal-to-noise ratio (SNR), the ADC32RF45 device delivers a noise spectral density of –155 dBFS/Hz as well as dynamic range and channel isolation over a large input frequency range. The buffered analog input with on-chip termination provides uniform input impedance across a wide frequency range and minimizes sample-and-hold glitch energy.

Each ADC channel may be connected to a dual-band, digital down-converter (DDC) with up to three independent, 16-bit numerically-controlled oscillators (NCOs) per DDC for phase-coherent frequency hopping. Additionally, the ADC is equipped with front-end peak and RMS power detectors and alarm functions to support external automatic gain control (AGC) algorithms.

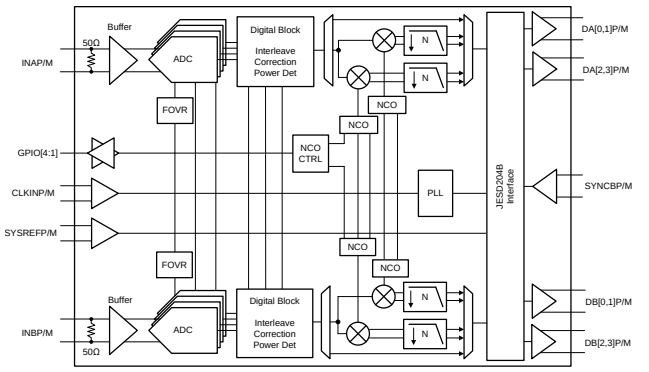
The ADC32RF45 device supports the JESD204B serial interface with subclass 1-based deterministic latency using data rates up to 12.3 Gbps with up to four lanes per ADC. The device is offered in a 72-pin VQFN package (10 mm × 10 mm) and supports the industrial temperature range (–40°C to +85°C).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADC32RF45	VQFN (72)	10.00 mm × 10.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram



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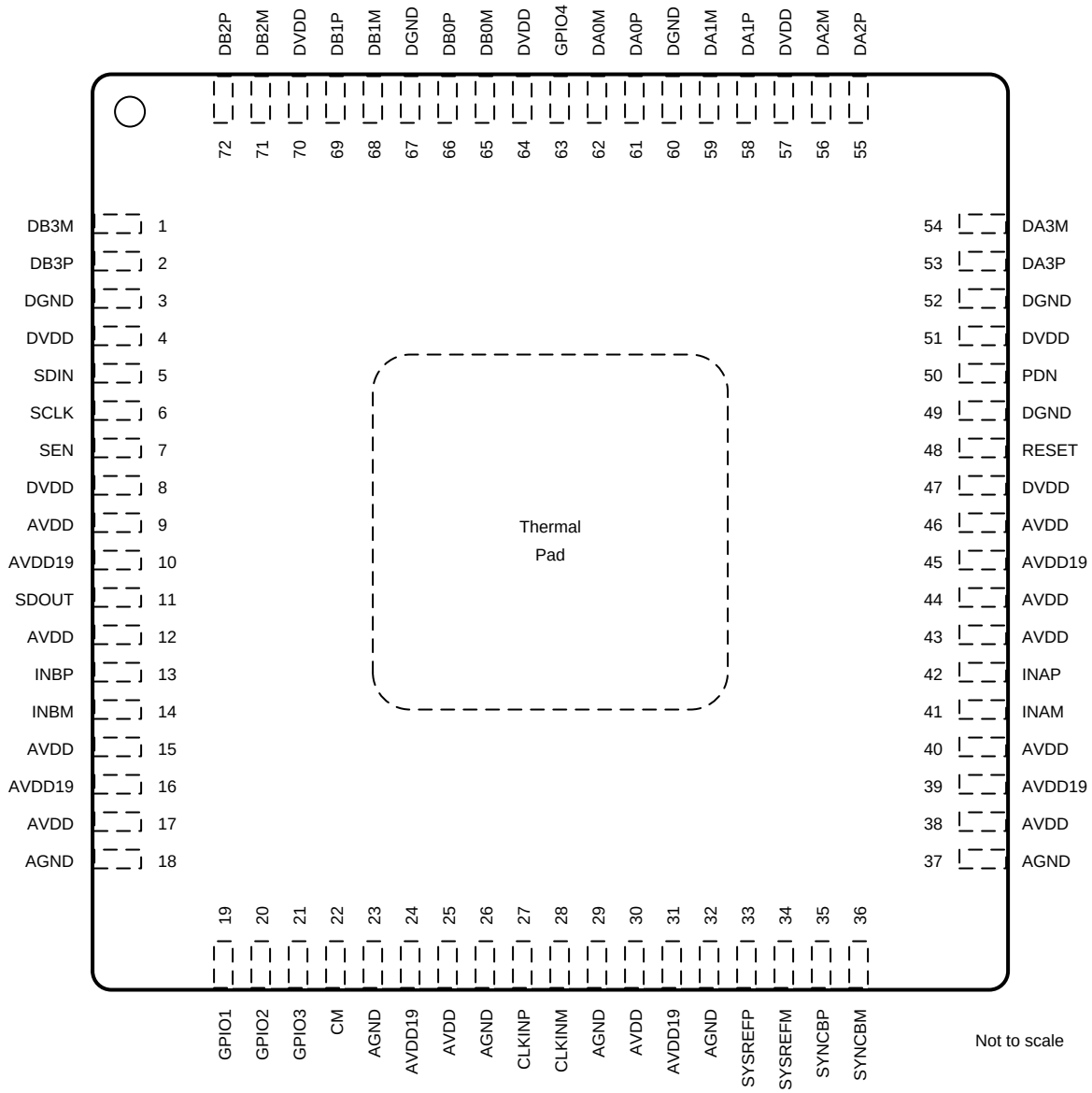
• Changed maximum values for applied input pin voltage in *Absolute Maximum Ratings* table	5
• Changed typical value for input capacitance parameter in *Electrical Characteristics* table	6
• Changed input capacitance test condition in *Electrical Characteristics* table	6
• Added "differential peak to peak" to input clock amplitude parameter in *Electrical Characteristics* table.	6
• Added *Parameter Measurement Information* section	15
• Updated Functional Block Diagram	16
• Added "with 100-Ω reference impedance" to Analog Inputs and Clock Input subsections of *Feature Description* section	17
• Added sentence to *Alarm Outputs: Power Detectors for AGC Support* subsection	34
• Changed number of active DDCS in *JESD Mode Options: Single-Band Real Output* table	51
• Changed hex value for Addresses 2D, 40 and 42 in *Address and Required Settings for the Initialization Registers* table	93
• Added description sentence and deleted comment in Step 1 in *Initialization Sequence* table	94
• Changed description value from 1.85 V to 1.9 V in *Initialization Sequence* table	94
• Reformatted links in *Related Documentation* section	102
• Added *Receiving Notification of Documentation Updates* section	102

5 Pin Configuration and Functions

RMP Package
72-Pin VQFN
Top View



Pin Functions

NAME	NO.	I/O	DESCRIPTION
INPUT, REFERENCE			
INAM	41	I	Differential analog input for channel A
INAP	42		
INBM	14	I	Differential analog input for channel B
INBP	13		
CM	22	O	Common-mode voltage for analog inputs, 1.4 V

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Pin Functions (continued)

NAME	NO.	I/O	DESCRIPTION
CLOCK, SYNC			
CLKINM	28	I	Differential clock input for the analog-to-digital converter (ADC). These pins have an internal differential 100-Ω termination.
CLKINP	27		
SYSREFM	34	I	External sync input. These pins have an internal, differential 100-Ω termination and require external biasing.
SYSREFP	33		
GPIO1	19	I/O	GPIO control pins; configured through SPI. This pin may be configured to be either a fast overrange output channel A and B, a fast detect alarm signal from the peak power detect, or a numerically-controlled oscillator (NCO) control. GPIO 4 (pin 63) may also be configured as a single-ended SYNCB input.
GPIO2	20		
GPIO3	21		
GPIO4	63		
CONTROL, SERIAL			
RESET	48	I	Hardware reset; active high. This pin has an internal 20-kΩ pulldown resistor.
SCLK	6	I	Serial interface clock input. This pin has an internal 20-kΩ pulldown resistor.
SDIN	5	I	Serial interface data input. This pin has an internal 20-kΩ pulldown resistor.
SEN	7	I	Serial interface enable. This pin has an internal 20-kΩ pullup resistor to DVDD.
SDOUT	11	O	Serial interface data output
PDN	50	I	Power down; active high. This pin may be configured through an SPI register setting and may be configured to a fast overrange output channel B through SPI. This pin has an internal 20-kΩ pulldown resistor.
DATA INTERFACE			
DA0M	62	O	JESD204B serial data output for channel A
DA0P	61		
DA1M	59		
DA1P	58		
DA2M	56		
DA2P	55		
DA3M	54		
DA3P	53		
DB0M	65	O	JESD204B serial data output for channel B
DB0P	66		
DB1M	68		
DB1P	69		
DB2M	71		
DB2P	72		
DB3M	1		
DB3P	2		
SYNCBM	36	I	Synchronization input for the JESD204B port. These pins have a LVDS or 1.8-V logic input, an optional on-chip 100-Ω termination, and is selectable through SPI. These pins require external biasing.
SYNCBP	35		
POWER SUPPLY			
AVDD19	10, 16, 24, 31, 39, 45	I	Analog 1.9-V power supply
AVDD	9, 12, 15, 17, 25, 30, 38, 40, 43, 44, 46	I	Analog 1.15-V power supply
DVDD	4, 8, 47, 51, 57, 64, 70	I	Digital 1.15 V-power supply, including the JESD204B transmitter
AGND	18, 23, 26, 29, 32, 37	I	Analog ground
DGND	3, 49, 52, 60, 67	I	Digital ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range	AVDD19	–0.3	2.1	V
	AVDD	–0.3	1.4	
	DVDD	–0.3	1.4	
Voltage between AGND and DGND		–0.3	0.3	V
Voltage applied to input pins	INAP, INAM and INBP, INBM	–0.3	AVDD19 + 0.3	V
	CLKINP, CLKINM	–0.3	AVDD + 0.6	
	SYSREFP, SYSREFM, SYNCBP, SYNCBM	–0.3	AVDD + 0.6	
	SCLK, SEN, SDIN, RESET, PDN, GPIO1, GPIO2, GPIO3, GPIO4	–0.2	AVDD19 + 0.2	
Temperature	Operating free-air, T_A	–40	85	°C
	Operating junction, T_J		**TBD**	
	Storage, T_{stg}	**TBD**	**TBD**	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	**TBD**	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage range	AVDD19	1.8	1.9	2.0	V
	AVDD	1.1	1.15	1.25	
	DVDD	1.1	1.15	1.2	
Temperature	Operating free-air, T_A	–40		85	°C
	Operating junction, T_J		105(1)	125	

(1) Prolonged use above this junction temperature may increase the device failure-in-time (FIT) rate.

6.4 Thermal Information

THERMAL METRIC(1)		ADC32RF45 RMP (VQFN) 72 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	21.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	4.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	2.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	2.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.2	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

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6.5 Electrical Characteristics

typical values are at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 3 GHz, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = 1.15 V, DVDD = 1.15 V, and –2-dBFS differential input (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DUAL-CHANNEL OPERATION						
I_{AVDD19}	1.9-V analog supply current	12-bit, bypass mode, f_S = 3.0 GSPS		1760		mA
		14-bit, bypass mode, f_S = 2.5 GSPS		1720		
		14-bit, bypass mode, f_S = 2.0 GSPS		1680		
I_{AVDD}	1.15-V analog supply current	12-bit, bypass mode, f_S = 3.0 GSPS		960		mA
		14-bit, bypass mode, f_S = 2.5 GSPS		860		
		14-bit, bypass mode, f_S = 2.0 GSPS		770		
I_{DVDD}	1.15-V digital supply current	12-bit, bypass mode, f_S = 3.0 GSPS		1700		mA
		14-bit, bypass mode, f_S = 2.5 GSPS		1460		
		14-bit, bypass mode, f_S = 2.0 GSPS		1230		
P_D	Power dissipation	12-bit, bypass mode, f_S = 3.0 GSPS		6.4		W
		14-bit, bypass mode, f_S = 2.5 GSPS		5.9		
		14-bit, bypass mode, f_S = 2.0 GSPS		5.5		
	Global power-down power dissipation			**TBD**		mW
SINGLE-CHANNEL OPERATION (One Channel Powered Down)						
I_{AVDD19}	1.9-V analog supply current	12-bit, bypass mode, f_S = 3.0 GSPS		960		mA
		14-bit, bypass mode, f_S = 2.5 GSPS		940		
		14-bit, bypass mode, f_S = 2.0 GSPS		920		
I_{AVDD}	1.15-V analog supply current	12-bit, bypass mode, f_S = 3.0 GSPS		520		mA
		14-bit, bypass mode, f_S = 2.5 GSPS		470		
		14-bit, bypass mode, f_S = 2.0 GSPS		420		
I_{DVDD}	1.15-V digital supply current	12-bit, bypass mode, f_S = 3.0 GSPS		1140		mA
		14-bit, bypass mode, f_S = 2.5 GSPS		1010		
		14-bit, bypass mode, f_S = 2.0 GSPS		840		
P_D	Power dissipation	12-bit, bypass mode, f_S = 3.0 GSPS		3.7		W
		14-bit, bypass mode, f_S = 2.5 GSPS		3.5		
		14-bit, bypass mode, f_S = 2.0 GSPS		3.2		
DUAL ADC OPERATION, DECIMATION ENABLED (f_S = 3.0 GSPS)						
I_{AVDD19}	1.9-V analog supply current			1750		mA
I_{AVDD}	1.15-V analog supply current			970		mA
I_{DVDD}	1.15-V digital supply current	4x decimation, single DDC		1760		mA
		8x decimation, single DDC		1730		
		8x decimation, dual DDC		1960		
		12x decimation, single DDC		**TBD**		
		12x decimation, dual DDC		**TBD**		
		16x decimation, single DDC		1690		
		16x decimation, dual DDC		1930		
		24x decimation, single DDC		**TBD**		
		24x decimation, dual DDC		**TBD**		
		32x decimation, single DDC		**TBD**		
		32x decimation, dual DDC		**TBD**		
P_D	Power dissipation	4x decimation, single DDC		6.4		W
		8x decimation, single DDC		6.4		
		8x decimation, dual DDC		6.7		

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Electrical Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 3 GHz, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = 1.15 V, DVDD = 1.15 V, and –2-dBFS differential input (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SINGLE ADC OPERATION, DECIMATION ENABLED (f_S = 3.0 GSPS, One Channel Powered Down)						
I_{AVDD19}	1.9-V analog supply current			**TBD**		mA
I_{AVDD}	1.15-V analog supply current			**TBD**		mA
I_{DVDD}	1.15-V digital supply current	4x decimation, single DDC		**TBD**		mA
		8x decimation, single DDC		**TBD**		
		8x decimation, dual DDC		**TBD**		
		16x decimation, single DDC		**TBD**		
		16x decimation, dual DDC		**TBD**		
		24x decimation, single DDC		**TBD**		
		24x decimation, dual DDC		**TBD**		
		32x decimation, single DDC		**TBD**		
		32x decimation, dual DDC		**TBD**		
P_D	Power dissipation	4x decimation, single DDC		**TBD**		W
		8x decimation, single DDC		**TBD**		
		8x decimation, dual DDC		**TBD**		
DUAL ADC OPERATION, DECIMATION ENABLED (f_S = 2.5 GSPS)						
I_{AVDD19}	1.9-V analog supply current			1710		mA
I_{AVDD}	1.15-V analog supply current			870		mA
I_{DVDD}	1.15-V digital supply current	4x decimation, single DDC		1550		mA
		10x decimation, single DDC		**TBD**		
		10x decimation, dual DDC		**TBD**		
		16x decimation, single DDC		**TBD**		
		20x decimation, single DDC		**TBD**		
		20x decimation, dual DDC		**TBD**		
P_D	Power dissipation	4x decimation, single DDC		6.0		W
		10x decimation, single DDC		**TBD**		
		10x decimation, dual DDC		**TBD**		
SINGLE ADC OPERATION, DECIMATION ENABLED (f_S = 2.5 GSPS, One Channel Powered Down)						
I_{AVDD19}	1.9-V analog supply current			**TBD**		mA
I_{AVDD}	1.15-V analog supply current			**TBD**		mA
I_{DVDD}	1.15-V digital supply current	4x decimation, single DDC		**TBD**		mA
		10x decimation, single DDC		**TBD**		
		10x decimation, dual DDC		**TBD**		
		16x decimation, single DDC		**TBD**		
		16x decimation, dual DDC		**TBD**		
		20x decimation, single DDC		**TBD**		
		20x decimation, dual DDC		**TBD**		
P_D	Power dissipation	4x decimation, single DDC		**TBD**		W
		10x decimation, single DDC		**TBD**		
		10x decimation, dual DDC		**TBD**		

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Electrical Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 3 GHz, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = 1.15 V, DVDD = 1.15 V, and –2-dBFS differential input (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
	ADC sampling rate		0.5	3.0		GSPS
	Resolution		14			Bits
	Differential input full-scale	With 50-Ω differential impedance		1.35		V_{PP}
				6.6		dBm
V_{IC}	Input common-mode voltage			1.4		V
C_o	Input resistance	Differential at dc		50		Ω
C_i	Input capacitance	Differential input to GND		2		pF
	V_{CM} common-mode voltage output			1.4		V
	Analog input bandwidth (3 dB)			3200		MHz
ISOLATION						
	Crosstalk isolation between channel A and channel B(1)	f_{IN} = 100 MHz		**TBD**		dBc
		f_{IN} = 900 MHz		99		
		f_{IN} = 1800 MHz		95		
		f_{IN} = 2700 MHz		TBD		
		f_{IN} = 3500 MHz		TBD		
CLOCK INPUT (2)						
	Input clock frequency		500	3000		MHz
	Differential (peak to peak) input clock amplitude		0.5	1.5	2.5	V_{PP}
	Input clock duty cycle		45%	50%	55%	
	Internal clock biasing			1.0		V
	Internal clock termination			100		Ω

(1) Crosstalk is measured with a –2-dBFS input signal on one channel and no input on the other channel.
(2) See *Input Clock Diagram*

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6.6 AC Performance Characteristics

typical values are at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 3 GHz, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = 1.15 V, DVDD = 1.15 V, and –2-dBFS differential input (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
SNR	Signal-to-noise ratio	f_{IN} = 100 MHz		61.8		dBFS
		f_{IN} = 900 MHz		60.6		
		f_{IN} = 1780 MHz		57.9		
		f_{IN} = 2100 MHz		57.2		
		f_{IN} = 2700 MHz		55.4		
		f_{IN} = 3500 MHz		54.7		
NSD	Noise spectral density averaged across the Nyquist zone	f_{IN} = 100 MHz		–153.6		dBFS/Hz
		f_{IN} = 900 MHz		–152.3		
		f_{IN} = 1780 MHz		–149.7		
		f_{IN} = 2100 MHz		–149.0		
		f_{IN} = 2700 MHz		–147.2		
		f_{IN} = 3500 MHz		–146.4		
	Small-signal SNR	A_{IN} = –40 dBFS		63.0		dBFS
NF	Input noise figure (1)	A_{IN} = –40 dBFS		24.7		dB
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 100 MHz		61.2		dBFS
		f_{IN} = 900 MHz		59.3		
		f_{IN} = 1780 MHz		57.1		
		f_{IN} = 2100 MHz		56.4		
		f_{IN} = 2700 MHz		55.0		
		f_{IN} = 3500 MHz		**TBD**		
ENOB	Effective number of bits	f_{IN} = 100 MHz		9.9		Bits
		f_{IN} = 900 MHz		9.6		
		f_{IN} = 1780 MHz		9.2		
		f_{IN} = 2100 MHz		9.1		
		f_{IN} = 2700 MHz		8.9		
		f_{IN} = 3500 MHz		**TBD**		
SFDR	Spurious-free dynamic range	f_{IN} = 100 MHz		71		dBc
		f_{IN} = 900 MHz		64		
		f_{IN} = 1780 MHz		63		
		f_{IN} = 2100 MHz		65		
		f_{IN} = 2700 MHz		55		
		f_{IN} = 3500 MHz		**TBD**		

(1) The ADC internal resistance = 65 Ω, driving source resistance = 50 Ω.

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AC Performance Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 3 GHz, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = 1.15 V, DVDD = 1.15 V, and –2-dBFS differential input (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
HD2	Second-order harmonic distortion	f_{IN} = 100 MHz		71		dBc
		f_{IN} = 900 MHz		75		
		f_{IN} = 1780 MHz		63		
		f_{IN} = 2100 MHz		65		
		f_{IN} = 2700 MHz		55		
		f_{IN} = 3500 MHz		**TBD**		
HD3	Third-order harmonic distortion	f_{IN} = 100 MHz		75		dBc
		f_{IN} = 900 MHz		64		
		f_{IN} = 1780 MHz		66		
		f_{IN} = 2100 MHz		68		
		f_{IN} = 2700 MHz		64		
		f_{IN} = 3500 MHz		**TBD**		
HD4, HD5	Fourth- and fifth-order harmonic distortion	f_{IN} = 100 MHz		77		dBc
		f_{IN} = 900 MHz		77		
		f_{IN} = 1780 MHz		79		
		f_{IN} = 2100 MHz		76		
		f_{IN} = 2700 MHz		69		
		f_{IN} = 3500 MHz		**TBD**		
IL spur	Interleaving spurs: $f_S / 2 – f_{IN}$, $f_S / 4 \pm f_{IN}$	f_{IN} = 100 MHz		87		dBc
		f_{IN} = 900 MHz		82		
		f_{IN} = 1780 MHz		79		
		f_{IN} = 2100 MHz		76		
		f_{IN} = 2700 MHz		77		
		f_{IN} = 3500 MHz		**TBD**		
HD2 IL	Interleaving spur for HD2: $f_S / 2 – HD2$	f_{IN} = 100 MHz		80		dBc
		f_{IN} = 900 MHz		80		
		f_{IN} = 1780 MHz		71		
		f_{IN} = 2100 MHz		70		
		f_{IN} = 2700 MHz		67		
		f_{IN} = 3500 MHz		**TBD**		
Worst spur	Spurious-free dynamic range (excluding HD2, HD3, HD4, HD5, and interleaving spurs IL and HD2 IL)	f_{IN} = 100 MHz		73		dBc
		f_{IN} = 900 MHz		72		
		f_{IN} = 1780 MHz		77		
		f_{IN} = 2100 MHz		75		
		f_{IN} = 2700 MHz		75		
		f_{IN} = 3500 MHz		**TBD**		
IMD3	Two-tone, third-order intermodulation distortion	f_1 = 850 MHz, f_2 = 900 MHz, A_{IN} = –10 dBFS		**TBD**		dBc
		f_1 = 1780 MHz, f_2 = 1790 MHz, A_{IN} = –10 dBFS		71		

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6.7 Digital Requirements

typical values are at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 3 GHz, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = 1.15 V, DVDD = 1.15 V, and –2-dBFS differential input (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
DIGITAL INPUTS (RESET, SCLK, SEN, SDIN, PDN, GPIO1, GPIO2, GPIO3, GPIO4)						
V_{IH}	High-level input voltage		0.8			V
V_{IL}	Low-level input voltage				0.4	V
I_{IH}	High-level input current			50		µA
I_{IL}	Low-level input current			–50		µA
C_i	Input capacitance			4		pF
DIGITAL OUTPUTS (SDOUT, GPIO1, GPIO2, GPIO3, GPIO4)						
V_{OH}	High-level output voltage		AVDD19 –0.1	AVDD19		V
V_{OL}	Low-level output voltage				0.1	V
DIGITAL INPUTS (SYNCBP, SYNCBM; Requires External Biasing)						
V_{ID}	Differential input voltage		350	450	1400	mV_{PP}
V_{CM}	Input common-mode voltage		**TBD**	1.2	**TBD**	V
DIGITAL INPUTS (SYSREFP, SYSREFM; Requires External Biasing)						
V_{ID}	Differential input voltage		350	450	1400	mV_{PP}
V_{CM}	Input common-mode voltage		1.15	1.2	1.25	V
DIGITAL OUTPUTS (JESD204B Interface: DA[3:0], DB[3:0], Meets JESD204B LV-0IF-11G-SR Standard)						
$\|V_{OD}\|$	Output differential voltage		**TBD**	700	**TBD**	mV_{PP}
$\|V_{OCM}\|$	Output common mode voltage			450		mV
	Transmitter short-circuit current	Transmitter terminals shorted to any voltage between –0.25 V and 1.45 V	–100		100	mA
z_{os}	Single-ended output impedance			50		Ω
C_o	Output capacitance	Output capacitance inside the device, from either output to ground		2		pF
	Internal input termination			100		Ω

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6.8 Timing Requirements

typical values are at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 3 GHz, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = 1.15 V, DVDD = 1.15 V, and –2-dBFS differential input (unless otherwise noted)

		MIN	NOM	MAX	UNIT
SAMPLE TIMING					
	Aperture delay		**TBD**		ns
	Aperture delay matching between two channels on the same device		**TBD**		ps
	Aperture delay matching between two devices at the same temperature and supply voltage		**TBD**		ps
	Aperture jitter, clock amplitude = 2 V_{PP}		70		f_S
	Wake-up timing coming out of global power-down		**TBD**		µs
	Data latency, ADC sample to digital output		**TBD**		Input clock cycles
	Fast overrange latency, ADC sample to FOVR indication on GPIO pins		**TBD**		Input clock cycles
t_{PD}	Propagation delay time: logic gates and output buffer delay (does not change with f_S)		**TBD**		ns
SYSREF TIMING					
t_{SU_SYSREF}	SYSREF setup time: referenced to clock rising edge, 3 GSPS	140	70		ps
t_{H_SYSREF}	SYSREF hold time: referenced to clock rising edge, 3 GSPS	50	20		ps
	Valid transition window sampling period: $t_{SU\_SYSREF} - t_{H\_SYSREF}$, 3 GSPS	143			ps
JESD OUTPUT INTERFACE TIMING					
UI	Unit interval: 12.3 Gbps	81.3	100		ps
	Rise, fall times: 1-pF single-ended load capacitance to ground		60		ps
	Total jitter: BER of 1E-15 and lane rate = 10 Gbps		26		ps
	Random jitter: BER of 1E-15 and lane rate = 10 Gbps		0.75		f_S rms
	Deterministic jitter: BER of 1E-15 and lane rate = 10 Gbps		12		ps, pk-pk
	Serial output data rate	2.5	10.0	12.3	Gbps

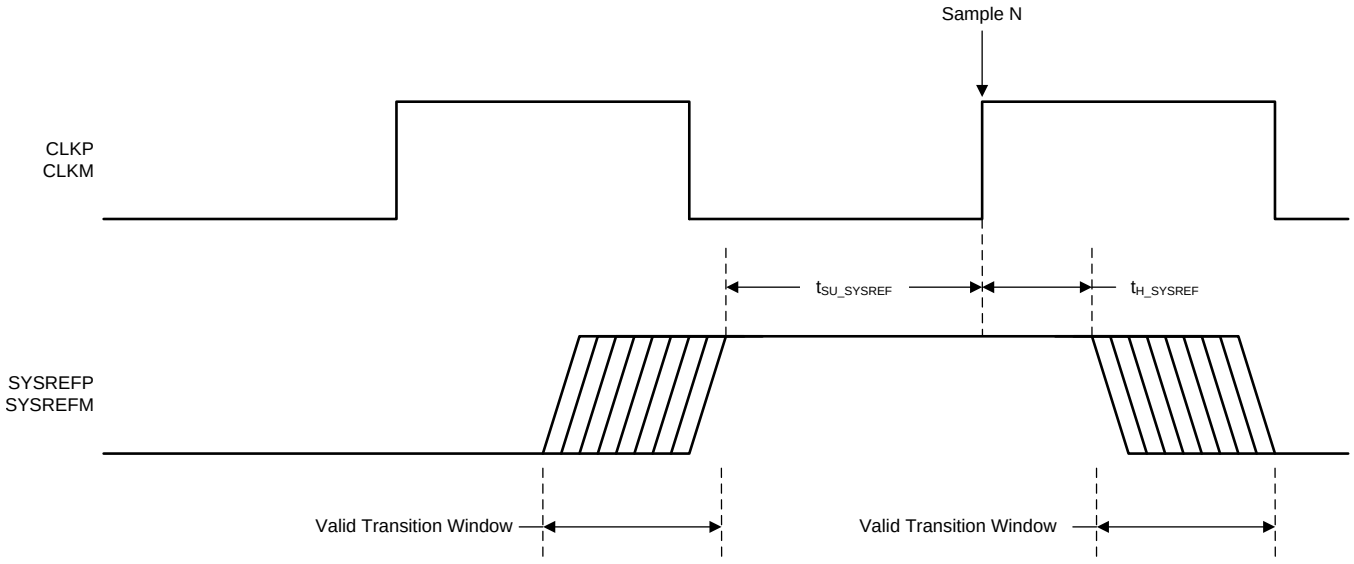

Figure 1. SYSREF Timing Diagram

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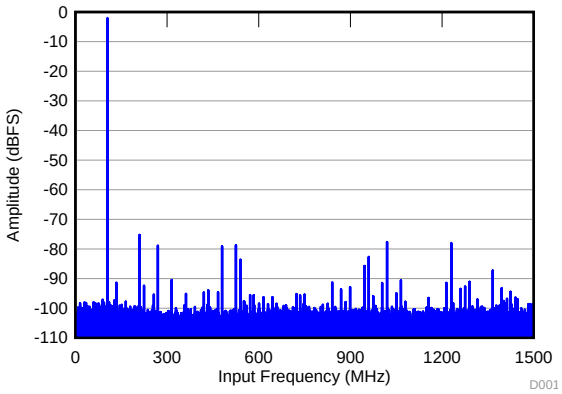
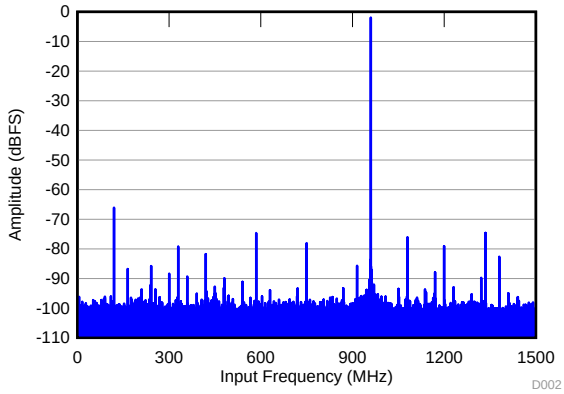
6.9 Typical Characteristics

typical values are at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 3 GHz, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = 1.15 V, DVDD = 1.15 V, and –2-dBFS differential input (unless otherwise noted)



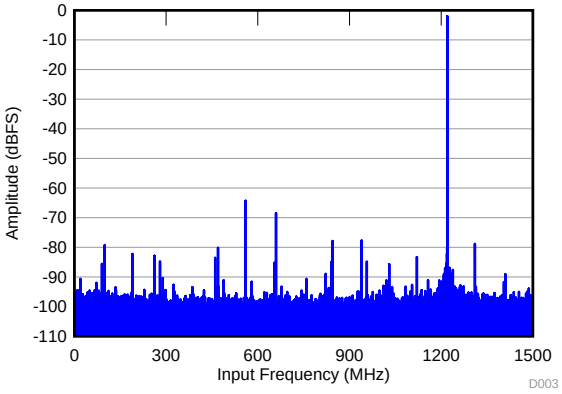
SNR = 61.8 dBFS; SFDR = 71 dBc;
HD2 = 71 dBc; HD3 = 75 dBc; HD4, HD5 = 77 dBc;
IL spur = 77 dBc; HD2_IL = 80 dBc; worst spur = 73 dBc

Figure 2. FFT for 100-MHz Input Frequency



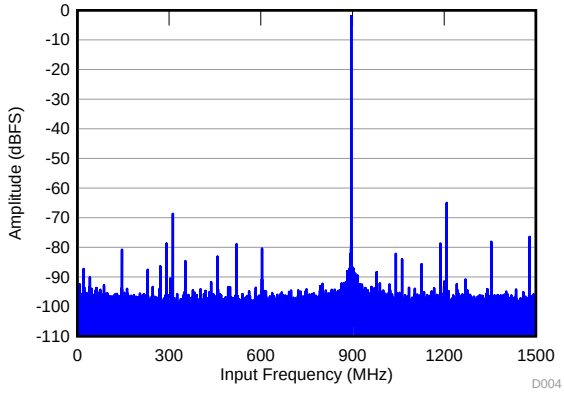
SNR = 60.6 dBFS; SFDR = 64 dBc;
HD2 = 75 dBc; HD3 = 64 dBc; HD4, HD5 = 77 dBc;
IL spur = 82 dBc; HD2_IL = 80 dBc; worst spur = 72 dBc

Figure 3. FFT for 900-MHz Input Frequency



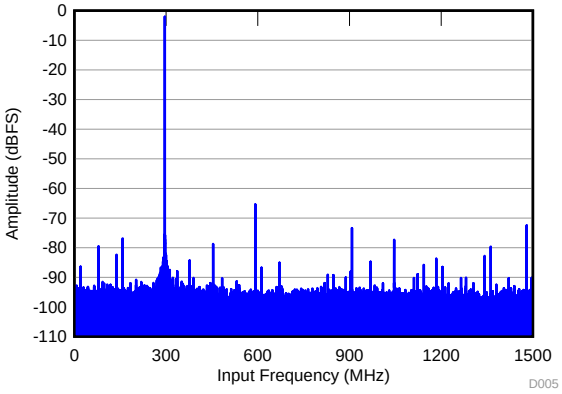
SNR = 57.9 dBFS; SFDR = 63 dBc;
HD2 = 63 dBc; HD3 = 66 dBc; HD4, HD5 = 79 dBc;
IL spur = 79 dBc; HD2_IL = 71 dBc; worst spur = 77 dBc

Figure 4. FFT for 1780-MHz Input Frequency



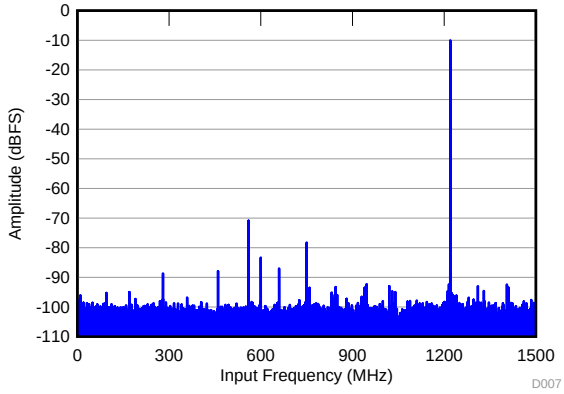
SNR = 57.2 dBFS; SFDR = 65 dBc;
HD2 = 65 dBc; HD3 = 68 dBc; HD4, HD5 = 76 dBc;
IL spur = 76 dBc; HD2_IL = 70 dBc; worst spur = 73 dBc

Figure 5. FFT for 2100-MHz Input Frequency



SNR = 55.4 dBFS; SFDR = 55 dBc;
HD2 = 55 dBc; HD3 = 64 dBc; HD4, HD5 = 69 dBc;
IL spur = 77 dBc; HD2_IL = 67 dBc; worst spur = 75 dBc

Figure 6. FFT for 2700-MHz Input Frequency



f_{IN} = 1.78 GHz, A_{IN} = –10 dBFS

Figure 7. FFT for 1780-MHz Input Frequency

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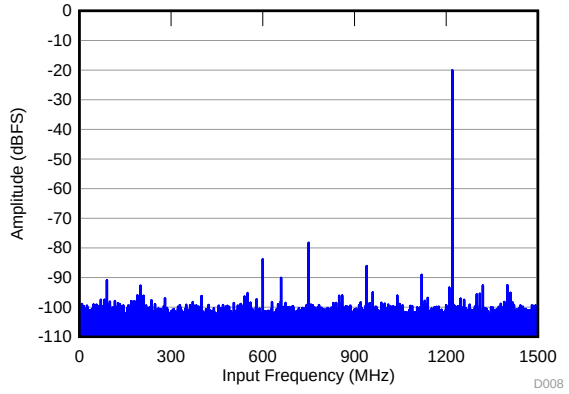
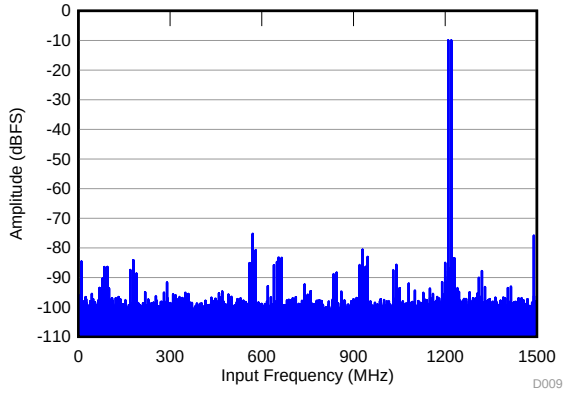
Typical Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 3 GHz, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = 1.15 V, DVDD = 1.15 V, and –2-dBFS differential input (unless otherwise noted)



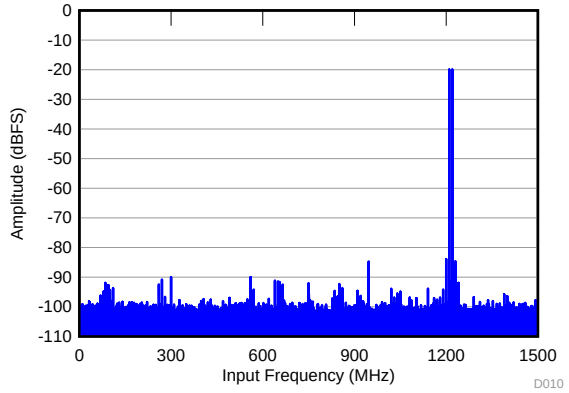
f_{IN} = 1.78 GHz, A_{IN} = –20 dBFS

Figure 8. FFT for 1780-MHz Input Frequency



f_{IN1} = 1770 MHz, f_{IN2} = 1790 MHz

Figure 9. Two-Tone FFT with –10 dBFS, Each Tone



f_{IN1} = 1770 MHz, f_{IN2} = 1790 MHz

Figure 10. Two-Tone FFT with –20 dBFS, Each Tone

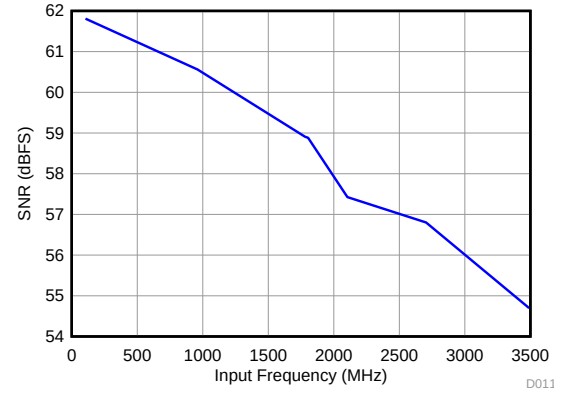


Figure 11. SNR vs Input Frequency

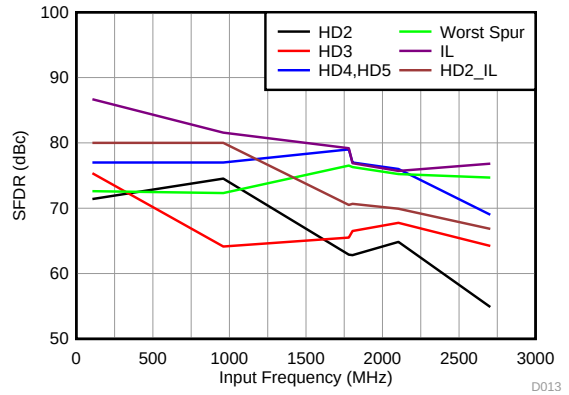


Figure 12. SFDR Performance vs Input Frequency

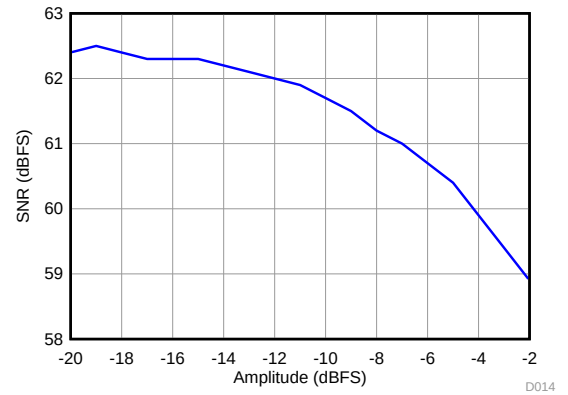


Figure 13. SNR vs Input Amplitude at 1.8-GHz Input Frequency

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Typical Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 3 GHz, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = 1.15 V, DVDD = 1.15 V, and –2-dBFS differential input (unless otherwise noted)

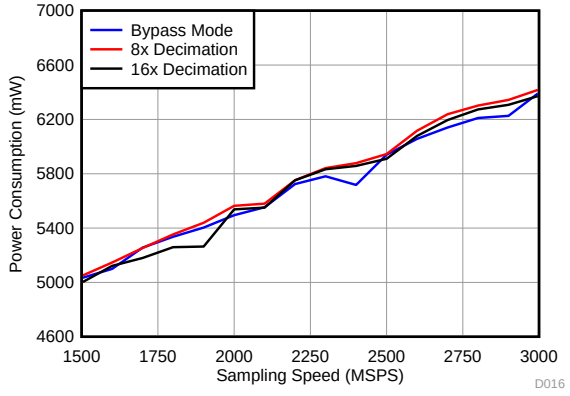


Figure 14. Power Consumption vs Sampling Rate

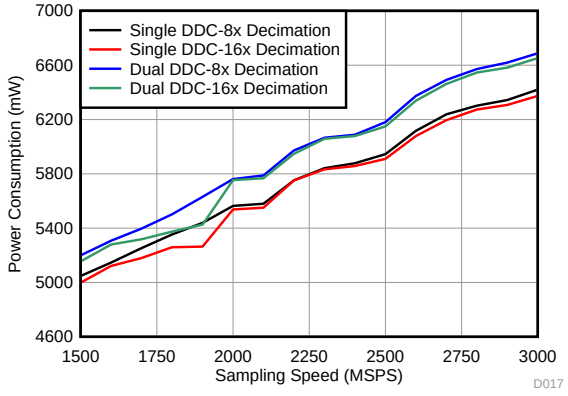
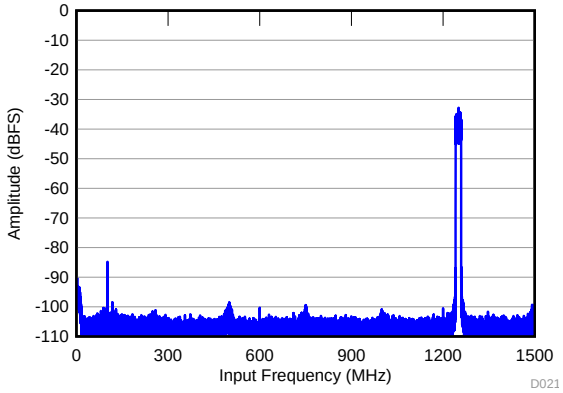


Figure 15. Power Consumption vs Sampling Rate



Carrier frequency = 1.75 GHz, bandwidth = 20 MHz

Figure 16. FFT with LTE Input

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7 Parameter Measurement Information

7.1 Input Clock Diagram

Figure 17 shows the input clock diagram.

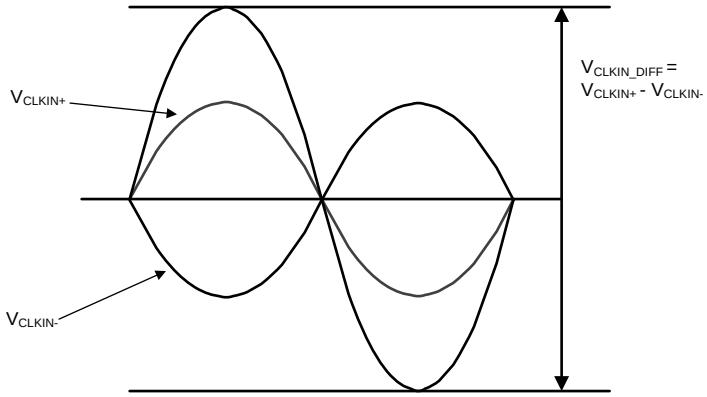


Figure 17. Input Clock Diagram

8 Detailed Description

8.1 Overview

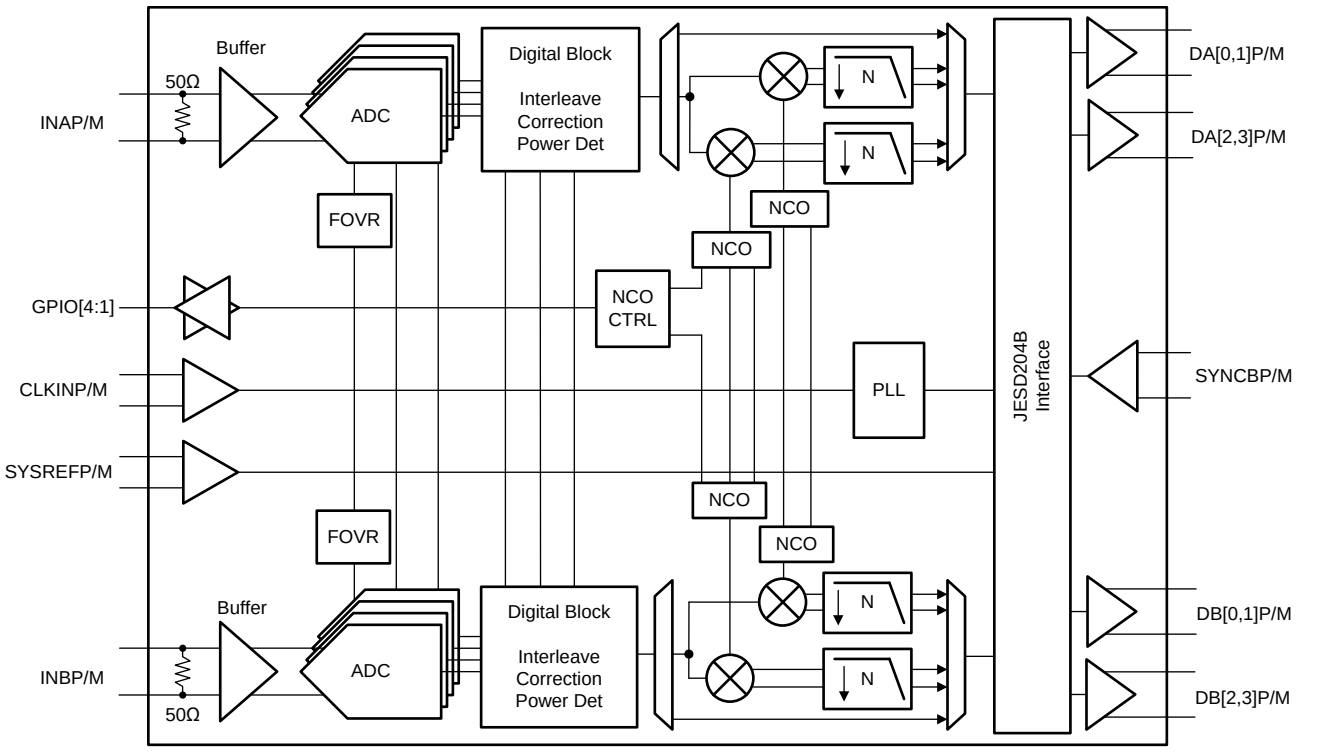
The ADC32RF45 device is a dual, 14-bit, 3-GSPS, analog-to-digital converter (ADC) followed by a multi-band digital down-converter (DDC) that may be bypassed, and a back-end JESD204B digital interface.

The ADCs are preceded by an input buffer and on-chip termination to provide a uniform input impedance over a large input frequency range. Furthermore, an internal differential clamping circuit provides first-level protection against overvoltage conditions. Each ADC channel is internally interleaved four times and equipped with background, analog and digital, and interleaving correction.

The on-chip DDC enables single- or dual-band internal processing to pre-select and filter smaller bands of interest and also reduces the digital output data traffic. Each DDC is equipped with up to three independent, 16-bit numerically-controlled oscillators (NCOs) for phase coherent frequency hopping; the NCOs may be controlled through the SPI or GPIO pins. The ADC32RF45 device also provides three different power detectors on-chip with alarm outputs in order to support external automatic gain control (AGC) loops.

The processed data are passed into the JESD204B interface where the data are framed, encoded, serialized, and output on one to four lanes per channel, depending on the ADC sampling rate and decimation. The CLKIN, SYSREF, and SYNCB inputs provide the device clock, SYSREF, and SYNCB signals to the JESD204B interface that are used to derive the internal local frame and local multi-frame clocks and establish the serial link. All features of the ADC32RF45 device are configurable through the 4-wire SPI.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Analog Inputs

The ADC32RF45 analog signal inputs are designed to be driven differentially. The analog input pins have internal analog buffers that drive the sampling circuit. The ADC32RF45 device provides on-chip, differential, 50-Ω termination to minimize reflections. The buffer also helps isolate the external driving circuit from the internal switching currents of the sampling circuit, thus resulting in a more constant SFDR performance across input frequencies.

The common-mode voltage of the signal inputs is internally biased to CM using the 25-Ω termination resistors that allow for ac-coupling of the input drive network. Figure 18 shows SDD11 at the analog inputs from dc to 5 GHz with 100-Ω reference impedance.

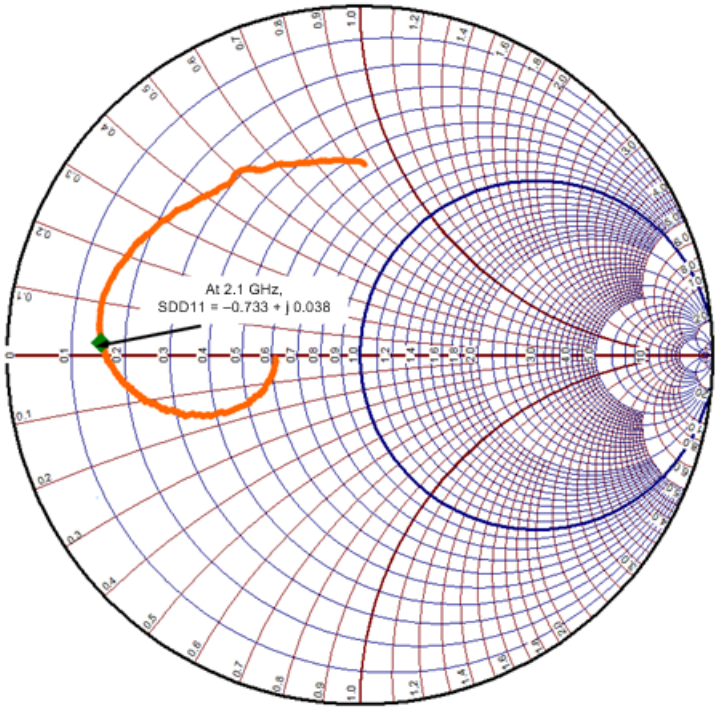


Figure 18. SDD11 Over Input Frequency Range

Feature Description (continued)

Each input pin (INP, INM) must swing symmetrically between (CM + 0.3375 V) and (CM – 0.3375 V), resulting in a 1.35-V_{PP} (default) differential input swing. The input sampling circuit has a 3-dB bandwidth that extends up to approximately 3.2 GHz, as shown in Figure 19.

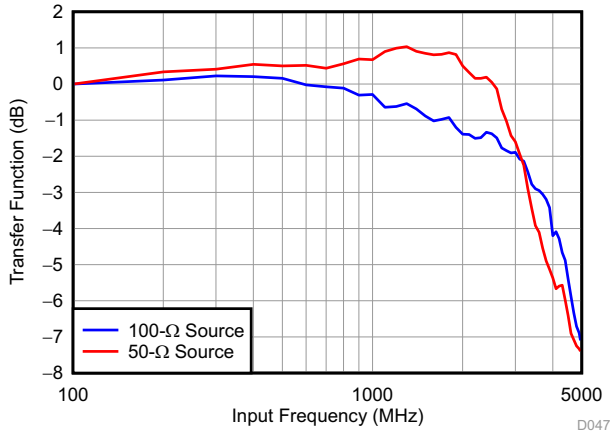


Figure 19. Input Bandwidth with 100-Ω Source Resistance

8.3.1.1 Input Clamp Circuit

The ADC32RF45 analog inputs include an internal, differential clamp for overvoltage protection. The clamp triggers for any input signals at approximately 600 mV above the input common-mode voltage, effectively limiting the maximum input signal to approximately 2.4 V_{PP}, as shown in Figure 20.

The maximum input current on each pin must be limited to approximately 20 mA.

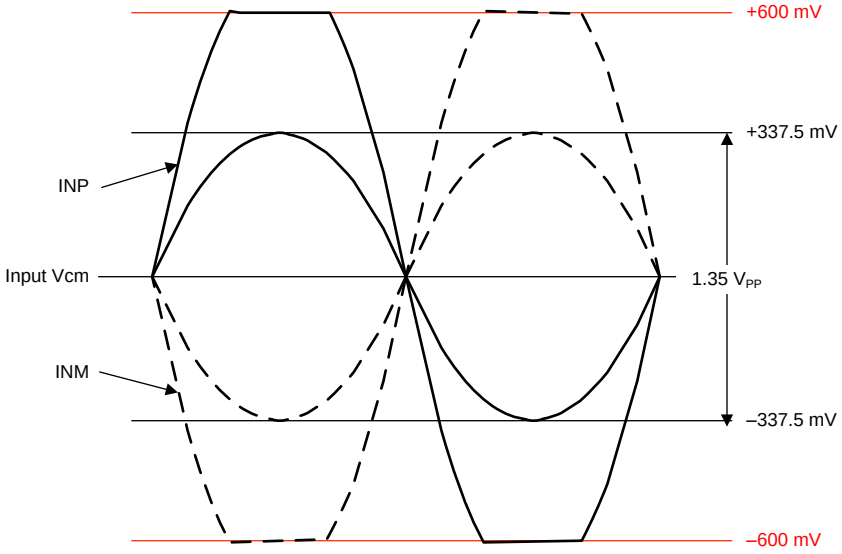


Figure 20. Clamp Response Timing Diagram

Feature Description (continued)

8.3.2 Clock Input

The ADC32RF45 sampling clock input includes internal 100-Ω differential termination along with on-chip biasing. The clock input is recommended to be ac-coupled externally. The input bandwidth of the clock input is approximately 3 GHz; the clock input impedance is illustrated with 100-Ω reference impedance in the smith chart of Figure 21.

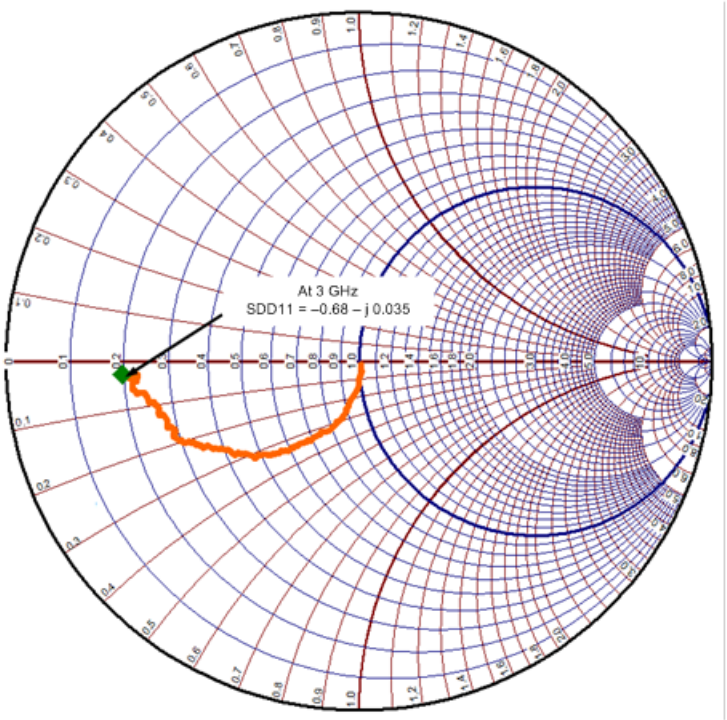


Figure 21. SDD11 of the Clock Input

The analog-to-digital converter (ADC) aperture jitter is a function of the clock amplitude applied to the pins. The equivalent aperture jitter for input frequencies at a 1-GHz and a 2-GHz input (f_S = 3 GSPS) is shown in Figure 22. Depending on the clock frequency, a matching circuit may be designed in order to maximize the clock amplitude.

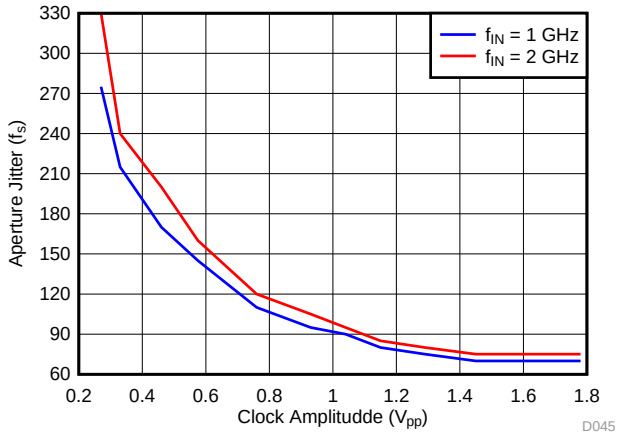


Figure 22. Equivalent Aperture Jitter vs Input Clock Amplitude

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Feature Description (continued)

8.3.3 SYSREF Input

The SYSREF signal is a periodic signal that is sampled by the ADC32RF45 device clock and is used to align the boundary of the local multiframe clock inside the data converter. SYSREF is also used to reset critical blocks [such as the clock divider for the interleaved ADCs, numerically-controlled oscillators (NCOs), decimation filters and so forth].

The SYSREF input requires external biasing. Furthermore, SYSREF must be established before the SPI registers are programmed. A programmable delay on the SYSREF input, as shown in Figure 23, is available to help with skew adjustment when the sampling clock and SYSREF are not provided from the same source.

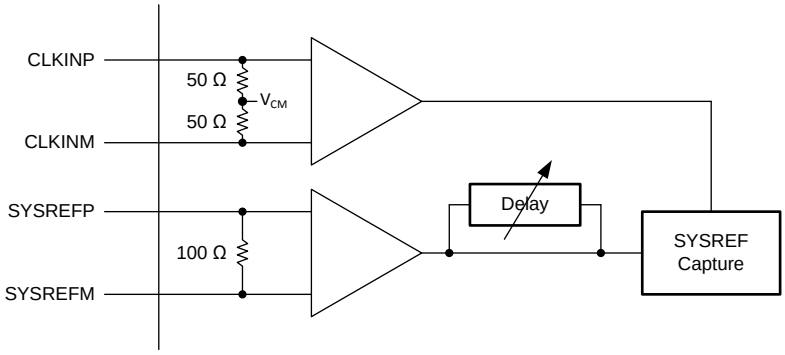

Figure 23. SYSREF Internal Circuit Diagram

8.3.3.1 SYSREF Timing

SYSREF is required to be a sub-harmonic of the internal local multiframe clock (LMFC), as described in Equation 1. Therefore, SYSREF is dependent on the device clock frequency and the LMFC frequency is determined by the selected decimation and frames per multiframe settings. The SYSREF signal is recommended to be a low-frequency signal less than 5 MHz in order to reduce coupling to the signal path both on the printed circuit board (PCB) as well as internal to the device.

SYSREF = LMFC / N (1)

where

- N is an integer value (1, 2, 3, and so forth)

In order for the interleaving correction engine to synchronize properly, the SYSREF frequency must also be a multiple of f_S / 64. Table 1 provides a summary of the valid LMFC clock settings.

Table 1. LMFC Clock Frequency Settings Overview

OPERATING MODE	LMFS SETTING	LMFC CLOCK
Bypass mode	82820, 42810	f_S / LCM (64, 20 × k)
Bypass mode	8224, 4211	f_S / LCM (64, k)
Decimation	Various	f_S / LCM (D, 64, k)

Example 1: f_S = 3.0 GSPS, Bypass Mode (LMFS = 82820), k = 16

SYSREF = 3.0 GSPS / LCM (64, 20 × 16) / N = 9.375 MHz / N

Operate SYSREF at 4.6875 MHz (effectively divide-by-640, N = 2)

Example 2: f_S = 3.0 GSPS, Divide-by-4, k = 16

SYSREF = 3.0 GSPS / LCM (4 ,64, 16) = 46.875 MHz / N

Operate SYSREF at 2.929688 MHz (effectively divide-by-1024, N = 16)

For proper device operation, disable the SYSREF signal after the JESD synchronization is established.

8.3.4 DDC Block

The ADC32RF45 device provides a sophisticated on-chip, digital down converter (DDC) block that may be controlled through SPI register settings and the general-purpose input/output (GPIO) pins. The DDC block supports two basic operating modes: receiver (RX) mode with single- or dual-band DDC and wide-bandwidth observation receiver mode.

Each ADC channel is followed by two DDC chains consisting of the digital filter along with a complex digital mixer with a 16-bit numerically-controlled oscillator (NCO), as shown in Figure 24. The NCOs allow accurate frequency tuning within the Nyquist zone prior to the digital filtering. One DDC chain is intended for supporting a dual-band DDC configuration in receiver mode and the second DDC chain supports the wide-bandwidth output option for the observation configuration. At any given time, either the single-band DDC, the dual-band DDC, or the wideband DDC may be enabled. Furthermore, three different NCO frequencies may be selected on that path and quickly switched using the SPI or the GPIO pins to enable wide-bandwidth observation in a multiband application.

Additionally, the decimation filter block provides the option to convert the complex output back to real format at double the 2x of the decimated, complex output rate. The filter response with a real output is identical to a complex output. The band is centered in the middle of the Nyquist zone (mixed with f_{OUT} / 4) based on a final output data rate of f_{OUT}.

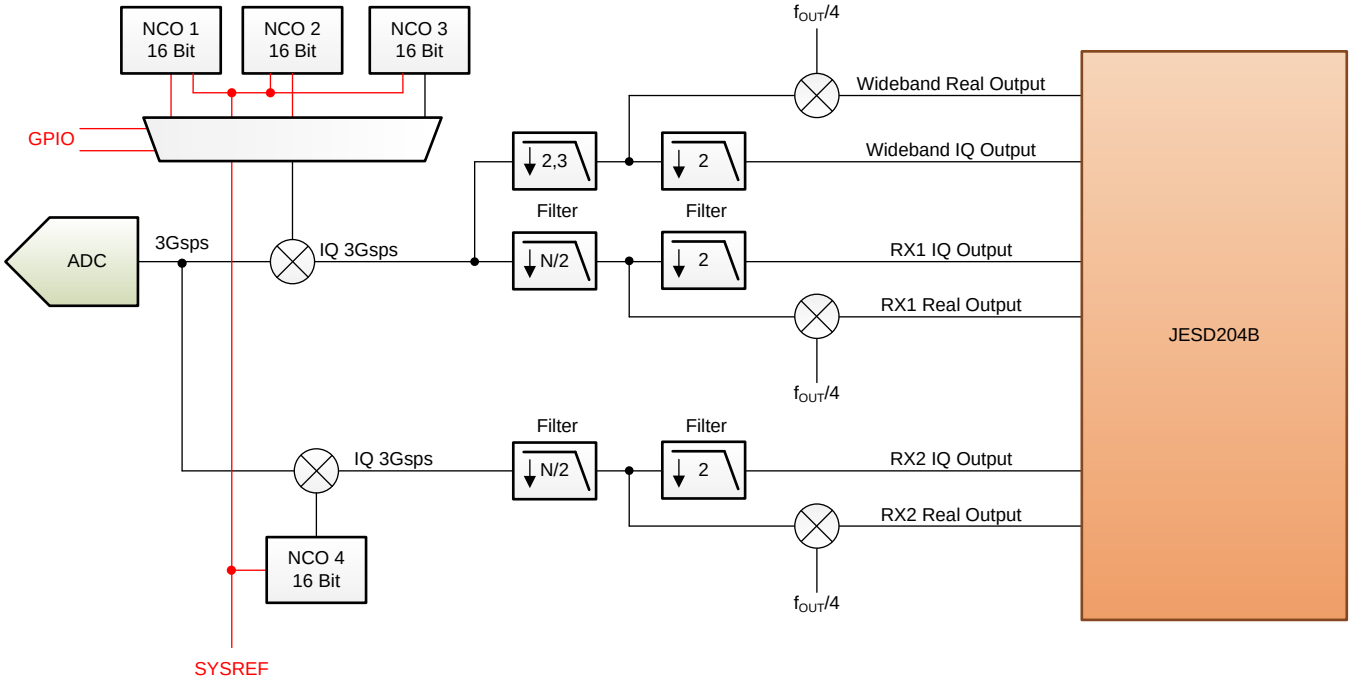

Figure 24. DDC Chains Overview (One ADC Channel Shown)

8.3.4.1 Operating Mode: Receiver

In receiver mode, the DDC block may be configured to single- or dual-band operation, as shown in Figure 25. Both DDC chains use the same decimation filter setting and the available options are discussed in the *Decimation Filters* section. The decimation filter setting also directly affects the interface rate and number of lanes of the JESD204B interface.

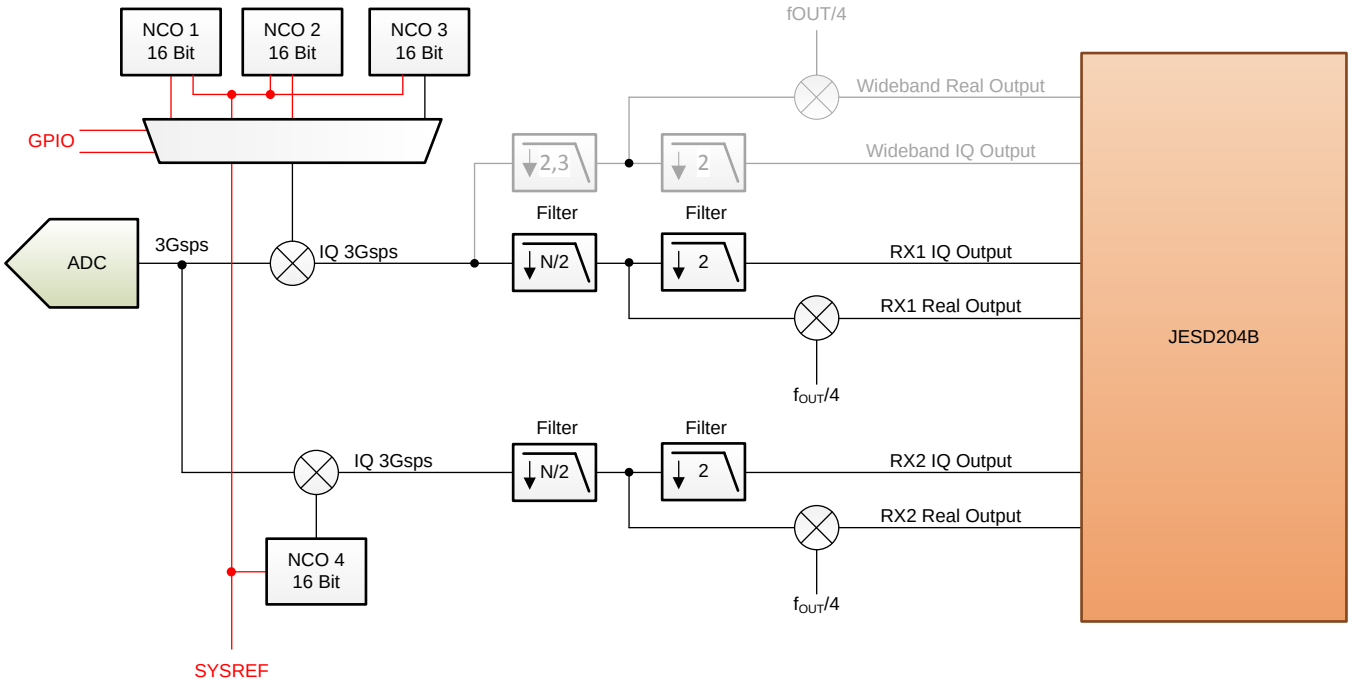

Figure 25. Decimation Filter Option for Single- or Dual-Band Operation

8.3.4.2 Operating Mode: Wide-Bandwidth Observation Receiver

This mode is intended for using a DDC with a wide bandwidth output, but for multiple bands. This mode uses a single DDC chain where up to three NCOs may be used to perform wide-bandwidth observation in a multiband environment, as shown in Figure 26. The three NCOs may be switched dynamically using either the GPIO pins or an SPI command. All three NCOs operate continuously to ensure phase continuity; however, when the NCO is switched, the output data are invalid until the decimation filters are completely flushed with data from the new band.

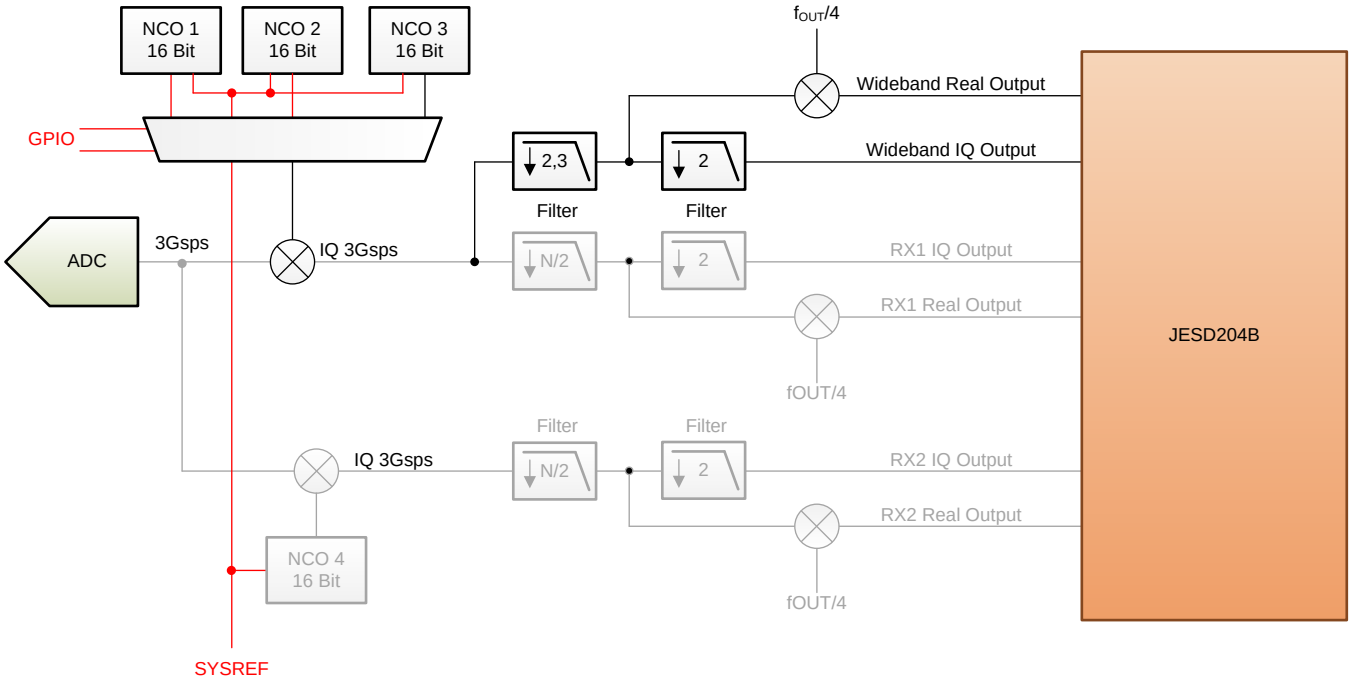

Figure 26. Decimation Filter Implementation for Single-Band and Wide-Bandwidth Mode

8.3.4.3 Decimation Filters

The stop-band rejection of the decimation filters is approximately 90 dB with a pass-band bandwidth of approximately 80%. Table 2 gives an overview of the pass-band bandwidth depending on decimation filter setting and ADC sampling rate.

Table 2. Decimation Filter Summary and Maximum Available Output Bandwidth

DECIMATION SETTING	NO. OF DDCS AVAILABLE PER CHANNEL	NOMINAL PASSBAND GAIN	BANDWIDTH		ADC SAMPLE RATE = N MSPS		ADC SAMPLE RATE = 3 GSPS	
			3 dB (%)	1 dB (%)	OUTPUT RATE (MSPS) PER BAND	OUTPUT BANDWIDTH (MHz) PER BAND	COMPLEX OUTPUT RATE (MSPS) PER BAND	OUTPUT BANDWIDTH (MHz) PER BAND
Divide-by-4 complex	1	–0.4 dB	90.9	86.8	N / 4 complex	0.4 × N / 2	750	600
Divide-by-6 complex	1	–0.65 dB	90.6	86.1	N / 6 complex	0.4 × N / 3	500	400
Divide-by-8 complex	2	–0.27 dB	91.0	86.8	N / 8 complex	0.4 × N / 4	375	300
Divide-by-9 complex	2	–0.45 dB	90.7	86.3	N / 9 complex	0.4 × N / 4.5	333.3	266.6
Divide-by-10 complex	2	–0.58 dB	90.7	86.3	N / 10 complex	0.4 × N / 5	300	240
Divide-by-12 complex	2	–0.55 dB	90.7	86.4	N / 12 complex	0.4 × N / 6	250	200
Divide-by-16 complex	2	–0.42 dB	90.8	86.4	N / 16 complex	0.4 × N / 8	187.5	150
Divide-by-18 complex	2	–0.83 dB	91.2	87.0	N / 18 complex	0.4 × N / 9	166.6	133
Divide-by-20 complex	2	–0.91 dB	91.2	87.0	N / 20 complex	0.4 × N / 10	150	120
Divide-by-24 complex	2	–0.95 db	91.1	86.9	N / 24 complex	0.4 × N / 12	125	100
Divide-by-32 complex	2	–0.78 dB	91.1	86.8	N / 32 complex	0.4 × N / 16	93.75	75

A dual-band example with a divide-by-8 complex is shown in Figure 27.

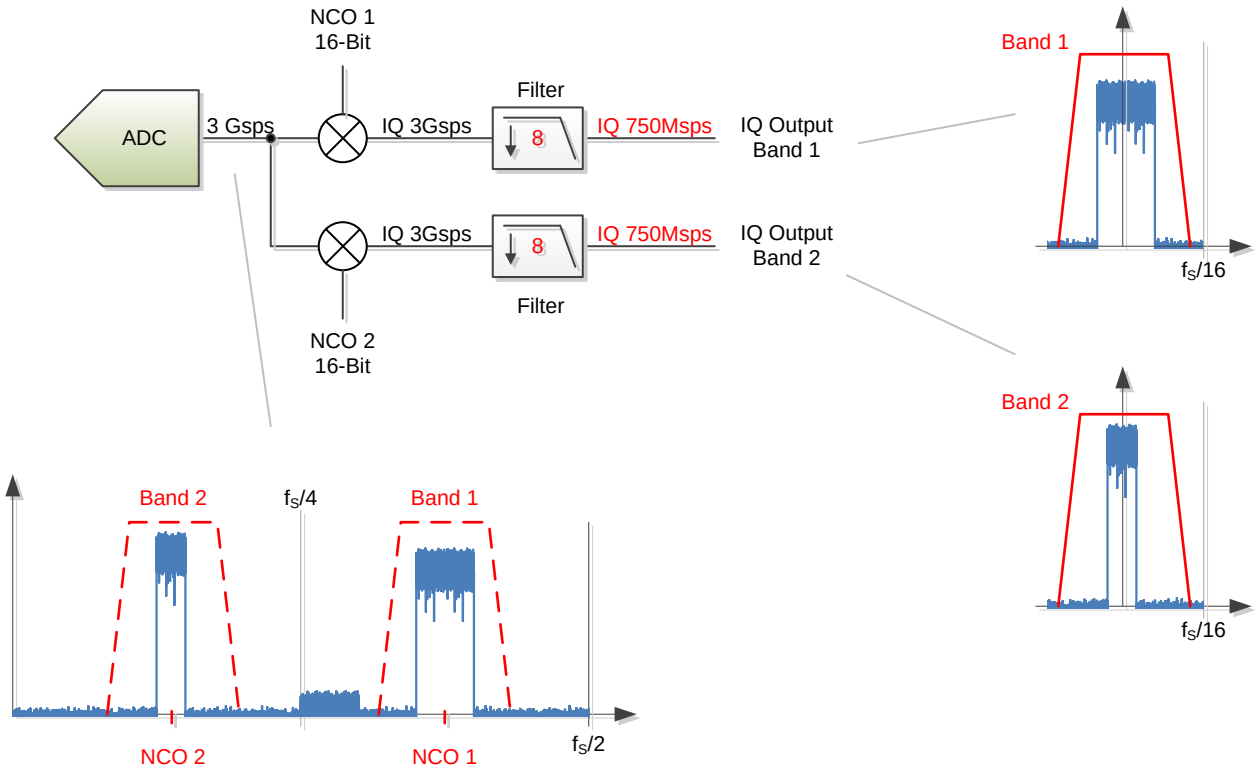

Figure 27. Dual-Band Example

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The decimation filter responses normalized to the ADC sampling clock are illustrated in Figure 27 to Figure 50 and may be interpreted as follows:

Each figure contains the filter passband, transition bands, and alias bands, as shown in Figure 28. The x-axis in Figure 28 shows the offset frequency (after the NCO frequency shift) normalized to the ADC sampling clock frequency.

For example, in the divide-by-4 complex, the output data rate is an f_S / 4 complex with a Nyquist zone of f_S / 8 or 0.125 × f_S. The transition band is centered around 0.125 × f_S and the alias transition band is centered at 0.375 × f_S. The alias bands that alias on top of the wanted signal band are centered at 0.25 × f_S and 0.5 × f_S (and are colored in red).

The decimation filters of the ADC32RF45 device provide greater than 90-dB attenuation for the alias bands.

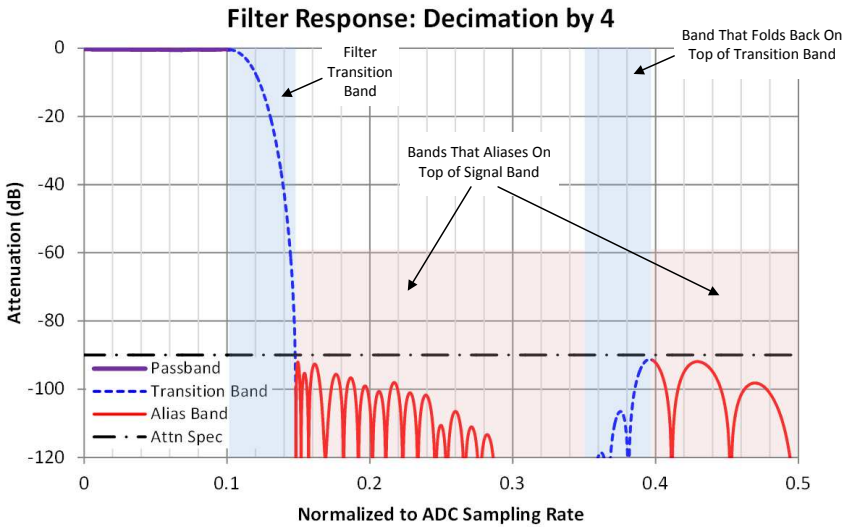

Figure 28. Interpretation of the Decimation Filter Plots

8.3.4.3.1 Divide-by-4

Peak-to-peak pass-band ripple: approximately 0.22 dB

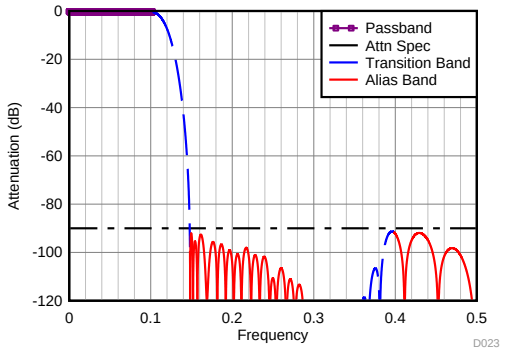

Figure 29. Divide-by-4 Filter Response

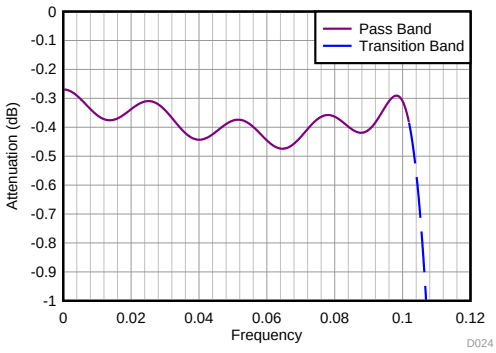

Figure 30. Divide-by-4 Filter Response (Zoomed)

8.3.4.3.2 Divide-by-6

Peak-to-peak pass-band ripple: approximately 0.38 dB

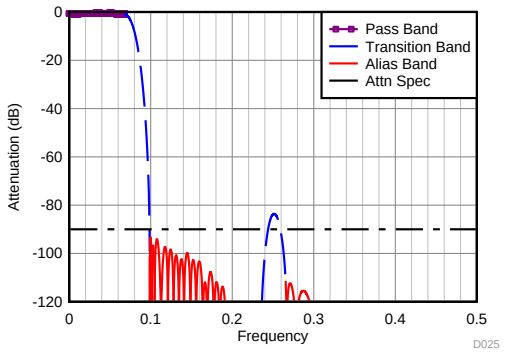

Figure 31. Divide-by-6 Filter Response

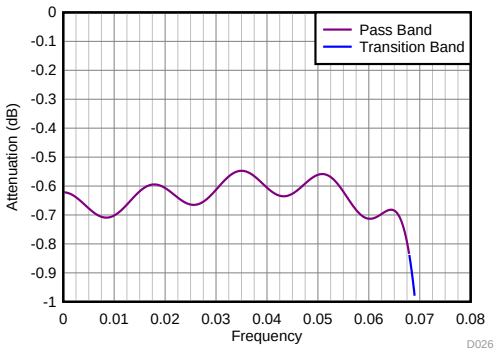

Figure 32. Divide-by-6 Filter Response (Zoomed)

8.3.4.3.3 Divide-by-8

Peak-to-peak pass-band ripple: approximately 0.25 dB

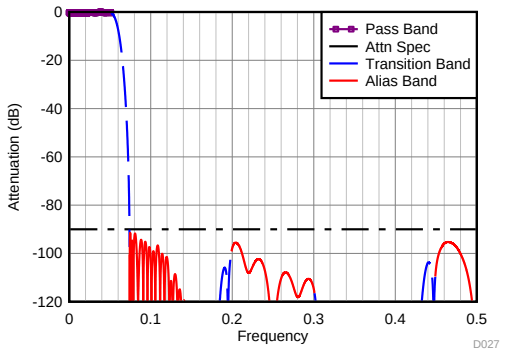

Figure 33. Divide-by-8 Filter Response

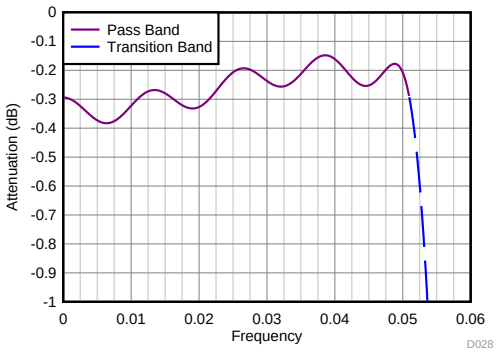

Figure 34. Divide-by-8 Filter Response (Zoomed)

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8.3.4.3.4 Divide-by-9

Peak-to-peak pass-band ripple: approximately 0.39 dB

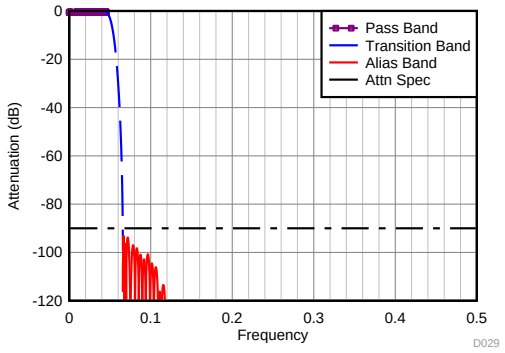

Figure 35. Divide-by-9 Filter Response

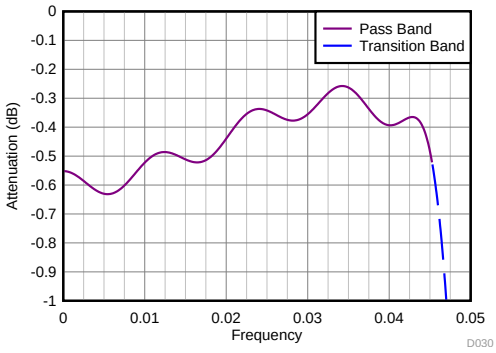

Figure 36. Divide-by-9 Filter Response (Zoomed)

8.3.4.3.5 Divide-by-10

Peak-to-peak pass-band ripple: approximately 0.39 dB

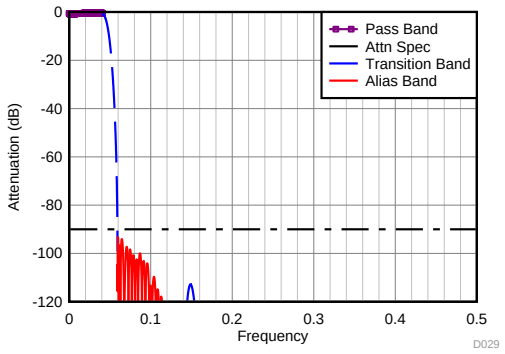

Figure 37. Divide-by-10 Filter Response

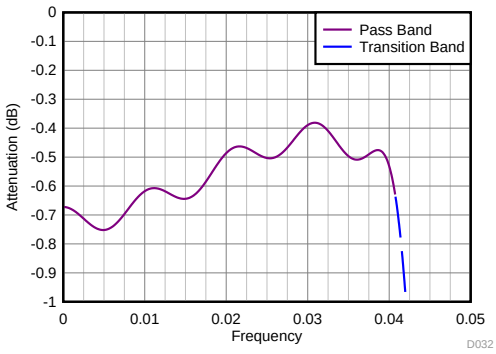

Figure 38. Divide-by-10 Filter Response (Zoomed)

8.3.4.3.6 Divide-by-12

Peak-to-peak pass-band ripple: approximately 0.36 dB

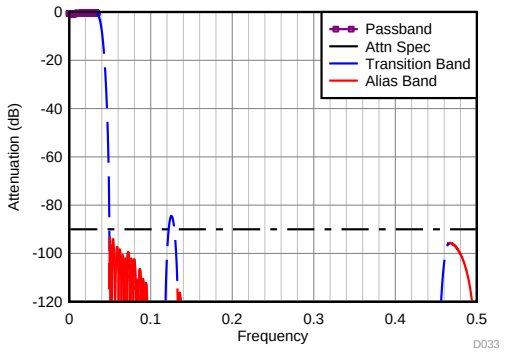

Figure 39. Divide-by-12 Filter Response

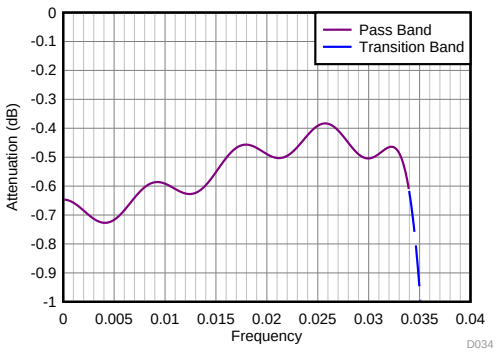

Figure 40. Divide-by-12 Filter Response (Zoomed)

8.3.4.3.7 Divide-by-16

Peak-to-peak pass-band ripple: approximately 0.29 dB

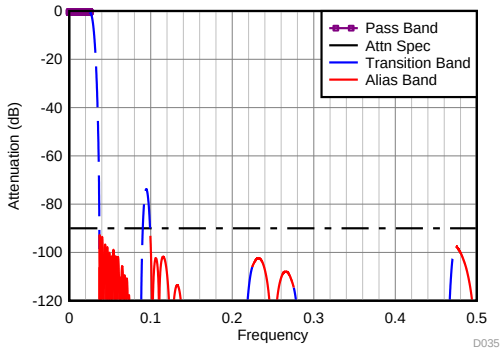

Figure 41. Divide-by-16 Filter Response

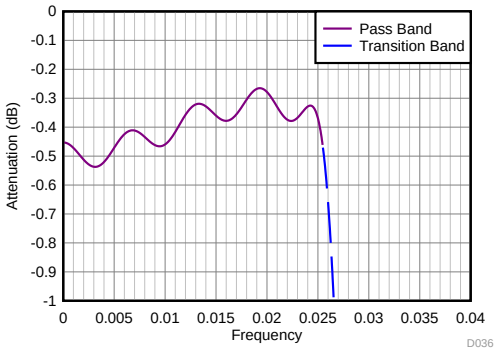

Figure 42. Divide-by-16 Filter Response (Zoomed)

8.3.4.3.8 Divide-by-18

Peak-to-peak pass-band ripple: approximately 0.33 dB

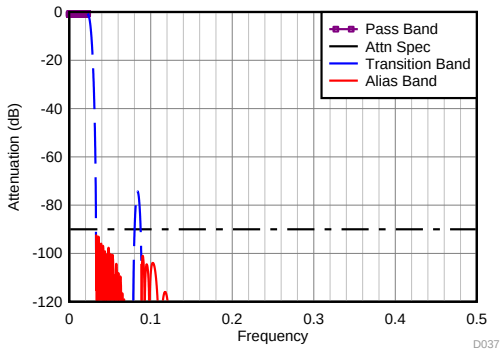

Figure 43. Divide-by-18 Filter Response

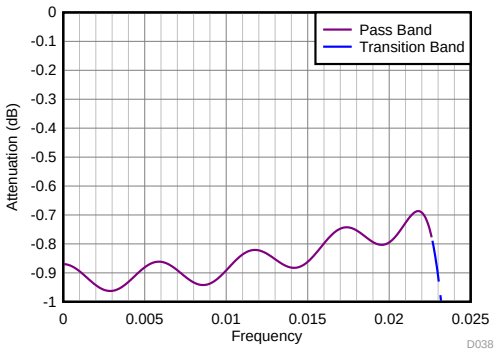

Figure 44. Divide-by-18 Filter Response (Zoomed)

8.3.4.3.9 Divide-by-20

Peak-to-peak pass-band ripple: approximately 0.32 dB

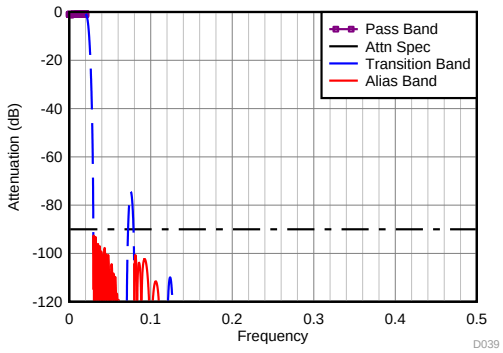

Figure 45. Divide-by-20 Filter Response

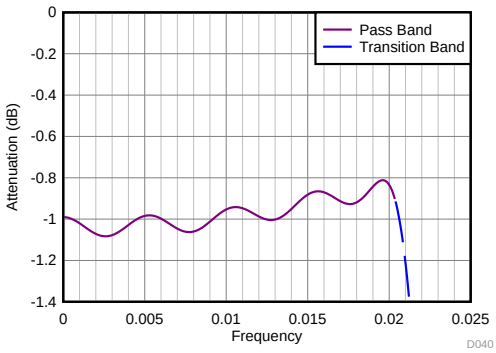

Figure 46. Divide-by-20 Filter Response (Zoomed)

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8.3.4.3.10 Divide-by-24

Peak-to-peak pass-band ripple: approximately 0.30 dB

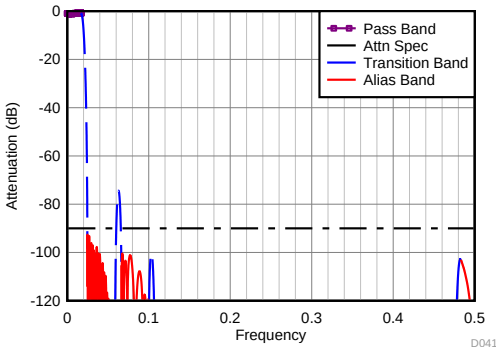

Figure 47. Divide-by-24 Filter Response

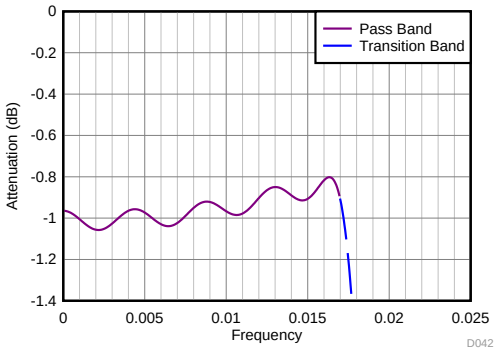

Figure 48. Divide-by-24 Filter Response (Zoomed)

8.3.4.3.11 Divide-by-32

Peak-to-peak pass-band ripple: approximately 0.24 dB

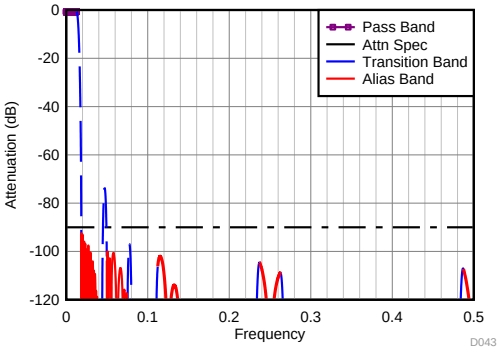

Figure 49. Divide-by-32 Filter Response

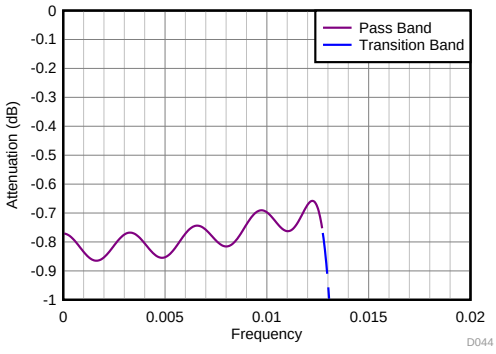

Figure 50. Divide-by-32 Filter Response (Zoomed)

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8.3.4.4 Digital Multiplexer (MUX)

The ADC32RF45 device supports a mode where the output data of ADC channel A may be routed internally to the digital blocks of both channel A and channel B. The ADC channel B may be powered down as shown in Figure 51. In this manner, the ADC32RF45 device may be configured as a single-channel ADC with up to four independent DDC chains or two wideband DDC chains. All decimation filters and JESD204B format configurations are identical to the two ADC channel operation.

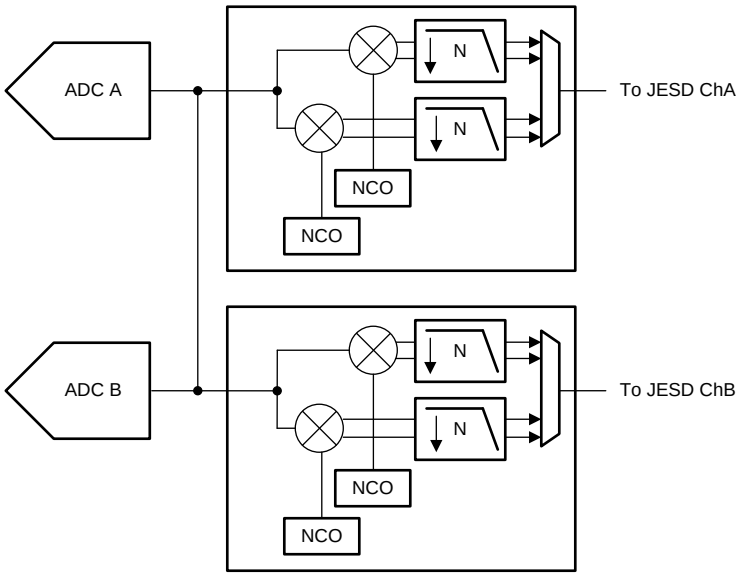

Figure 51. Digital Multiplexer Option

8.3.4.5 Numerically-Controlled Oscillators (NCOs) and Mixers

The ADC32RF45 device is equipped with three independent, complex NCOs per ADC channel. The oscillator generates a complex exponential sequence, as shown in Equation 2.

$$x[n] = e^{-j\omega n} \quad (2)$$

where

- frequency (ω) is specified as a signed number by the 16-bit register setting

The complex exponential sequence is multiplied by the real input from the ADC to mix the desired carrier down to 0 Hz.

Each ADC channel has two DDCs. The first DDC has three NCOs and the second DDC has one NCO. The first DDC may dynamically select one of the three NCOs based on the GPIO pin or SPI selection. In wide-bandwidth mode (lower decimation factors, for example, 4 and 6), there may only be one DDC for each ADC channel. The NCO frequencies may be programmed independently through the DDCx, NCO[4:1], and the MSB and LSB register settings.

The NCO frequency setting is set by the 16-bit register value given by Equation 3:

$$f_{NCO} = \frac{\left(DDCxNCOy - 2^{16}\right) \times f_S}{2^{16}} \quad (3)$$

where

- x = 0, 1
- y = 1 to 4

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For example:

If f_S = 3 GSPS, then the NCO register setting = 38230 (decimal).

Thus, f_{NCO} is defined by Equation 4:

$$f_{NCO} = \left(38230 - 2^{16}\right) \times \frac{3\ \text{GSPS}}{2^{16}} = -1249.97\ \text{MHz} \quad (4)$$

Any register setting changes that occur after the JESD204B interface is operational results in a non-deterministic NCO phase. If a deterministic phase is required, the JESD204B interface must be reinitialized after changing the register setting.

In bypass mode (when decimation filters are not used), the NCOs are powered down in order to avoid creating unwanted spurs.

8.3.5 NCO Switching

The first DDC (DDC0) on each ADC channel provides three different NCOs that may be used for phase-coherent frequency hopping. This feature is available in both single-band and dual-band mode, but only affects DDC0.

The NCOs may be switched through an SPI control or by using the GPIO pins with the register configurations shown in Table 3 for channel A (50xxh) and channel B (58xxh). The assignment of which GPIO pin to use for INSEL0 and INSEL1 is done based on Table 4 using registers 5438h and 5C38h. The NCO selection is done based on the logic selection on the GPIO pins, as shown in Table 5.

Table 3. NCO Register Configurations

REGISTER	ADDRESS	DESCRIPTION
NCO CONTROL THROUGH GPIO PINS		
NCO SEL Pin	500Fh, 580Fh	Selects the NCO control through the SPI (default) or a GPIO pin.
INSEL0, INSEL1	5438h, 5C38h	Selects which two GPIO pins are used to control the NCO.
NCO CONTROL through SPI CONTROL		
NCO SEL Pin	500Fh, 580Fh	Selects the NCO control through the SPI (default) or a GPIO pin.
NCO SEL	5010h, 5810h	Selects which NCO to use for DDC0.

Table 4. GPIO Pin Assignment

INSEL0 AND INSEL1	GPIO PIN SELECTED
00	GPIO4
01	GPIO1
10	GPIO3
11	GPIO2

Table 5. NCO Selection

INSEL1	INSEL0	NCO SELECTED
0	0	NCO1
0	1	NCO2
1	0	NCO3
1	1	n/a

8.3.6 CML SerDes Transmitter Interface

Each 12.3-Gbps serializer, deserializer (SerDes) CML transmitter output requires ac-coupling between the transmitter and receiver. Terminate the differential pair with 100-Ω resistance (that is, two 50-Ω resistors) as close to the receiving device as possible to avoid unwanted reflections and signal degradation, as shown in Figure 52.

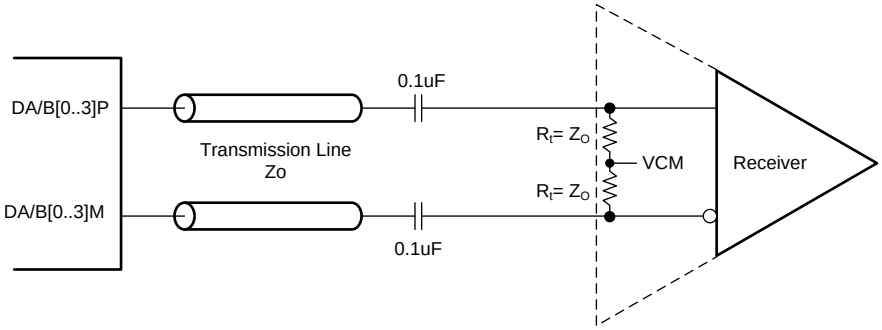

Figure 52. External Serial JESD204B Interface Connection

8.3.7 Eye Diagrams

Figure 53 and Figure 54 show the serial output eye diagrams of the ADC32RF45 device at 5.0 Gbps and 12 Gbps against the JESD204B mask.

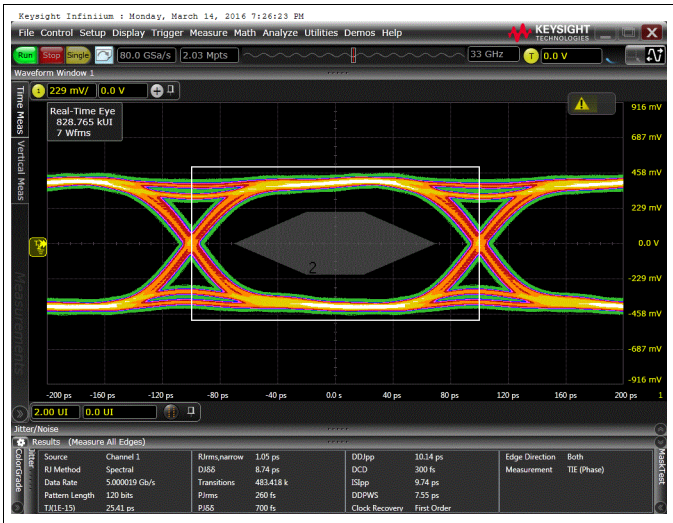

Figure 53. Data Eye at 5 Gbps

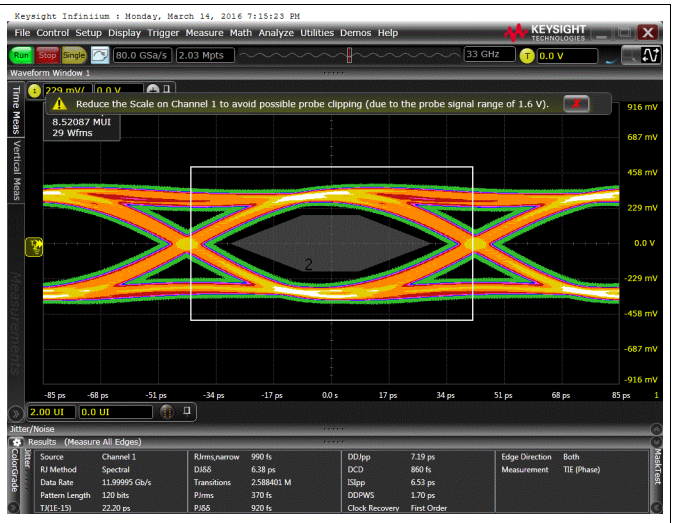

Figure 54. Data Eye at 12 Gbps

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8.3.8 Alarm Outputs: Power Detectors for AGC Support

The GPIO pins may be configured as alarm outputs for channels A and B. The ADC32RF45 device supports three different power detectors (an absolute peak power detector, crossing detector, and RMS power detector) as well as fast overrange from the ADC. The power detectors operate off full rate ADC output prior to the decimation filters.

8.3.8.1 Absolute Peak Power Detector

In this detector mode the peak is computed over eight samples of the ADC output. Next, the peak for a block of N samples (N × S`) is computed over a programmable block length and then compared against a threshold to either set or reset the peak detector output (Figure 55 and Figure 56). There are two sets of thresholds and each set has two thresholds for hysteresis. The programmable dwell-time counter is used for clearing the block detector alarm output.

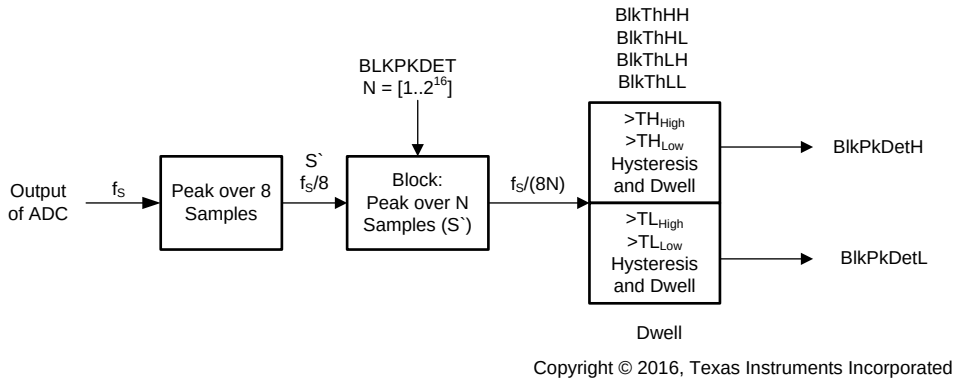

Figure 55. Peak Power Detector Implementation

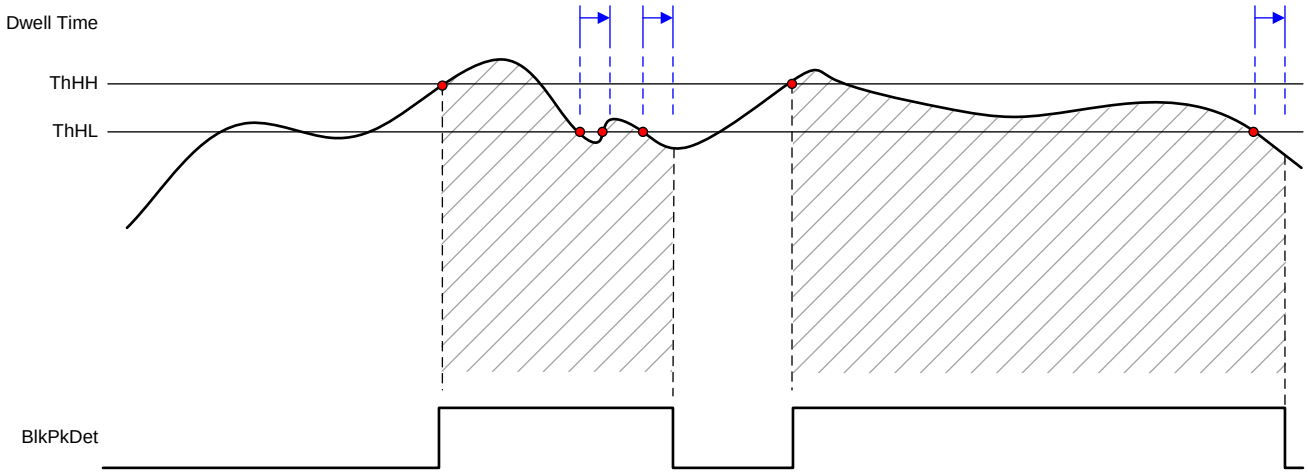

Figure 56. Peak Power Detector Timing Diagram

Table 6 shows the register configurations required to set up the absolute peak power detector. The detector operates in the f_S / 8 clock domain; one peak sample is calculated over eight actual samples.

The automatic gain control (AGC) modes may be configured separately for channel A (54xxh) and channel B (5Cxxh), although some registers are common in 54xxh (such as the GPIO pin selection).

Table 6. Registers Required for the Peak Power Detector

REGISTER	ADDRESS	DESCRIPTION
PKDET EN	5400, 5C00h	Enables peak detector
BLKPKDET	5401h, 5402h, 5403h, 5C01h, 5C02h, 5C03h	Sets the block length N of number of samples (S`). Number of actual ADC samples is 8x this value: N is 17 bits: 1 to 2^{16}.
BLKTHHH, BLKTHHL, BLKTHLH, BLKTHLL	5407h, 5408h, 5409h, 540Ah, 5C07h, 5C08h, 5C09h, 5C0Ah	Sets the different thresholds for the hysteresis function values from 0 to 256 (where 256 is equivalent to the peak amplitude). For example: if BLKTHHH is to –2 dBFS from peak, $10^{(-2 / 20)} \times 256 = 203$, then set 5407h and 5C07h = CBh.
DWELL	540Bh, 540Ch, 5C0Bh, 5C0Ch	When the computed block peak crosses the upper thresholds BLKTHHH or BLKTHLH, the peak detector output flags are set. In order to be reset, the computed block peak must remain continuously lower than the lower threshold (BLKTHHL or BLKTHLL) for the period specified by the DWELL value. This threshold is 16 bits and is specified in terms of f_S / 8 clock cycles.
OUTSEL GPIO[4:1]	5432h, 5433h, 5434h, 5435h	Connects the BLKPKDETH, BLKPKDETL alarms to the GPIO pins; common register.
IODIR	5437h	Selects the direction for the four GPIO pins; common register.
RESET AGC	542Bh, 5C2Bh	After configuration, reset the AGC module to start operation.

8.3.8.2 Crossing Detector

In this detector mode the peak is computed over eight samples of the ADC output. Next, the peak for a block of N samples (N × S`) is computed over a programmable block length and then the peak is compared against two sets of programmable thresholds (with hysteresis). The crossing detector counts how many f_S / 8 clock cycles that the block detector outputs are set high over a programmable time period and compares the counter value against the programmable thresholds. The alarm outputs are updated at the end of the time period, routed to the GPIO pins, and held in that state through the next cycle, as shown in Figure 57 and Figure 58. Alternatively, a 2-bit format may be used but (because the ADC32RF45 device has four GPIO pins available) this feature uses all four pins for a single channel.

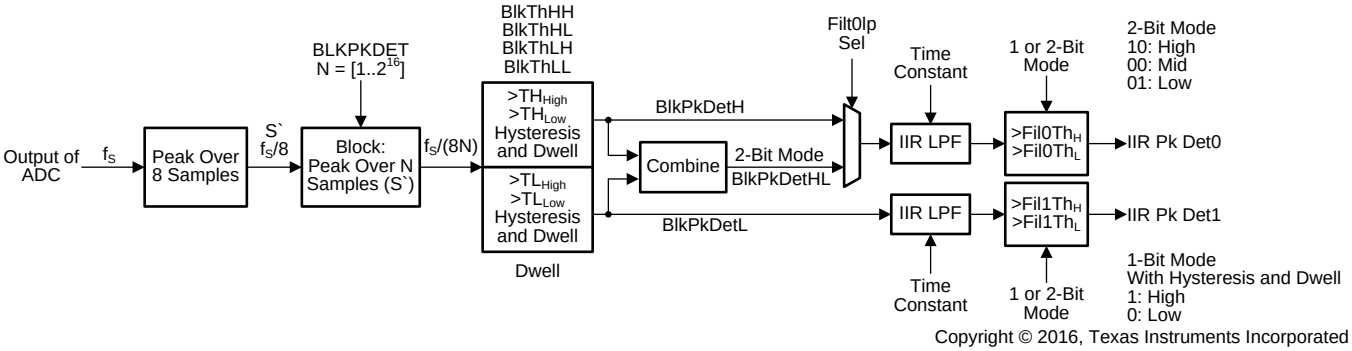

Figure 57. Crossing Detector Implementation

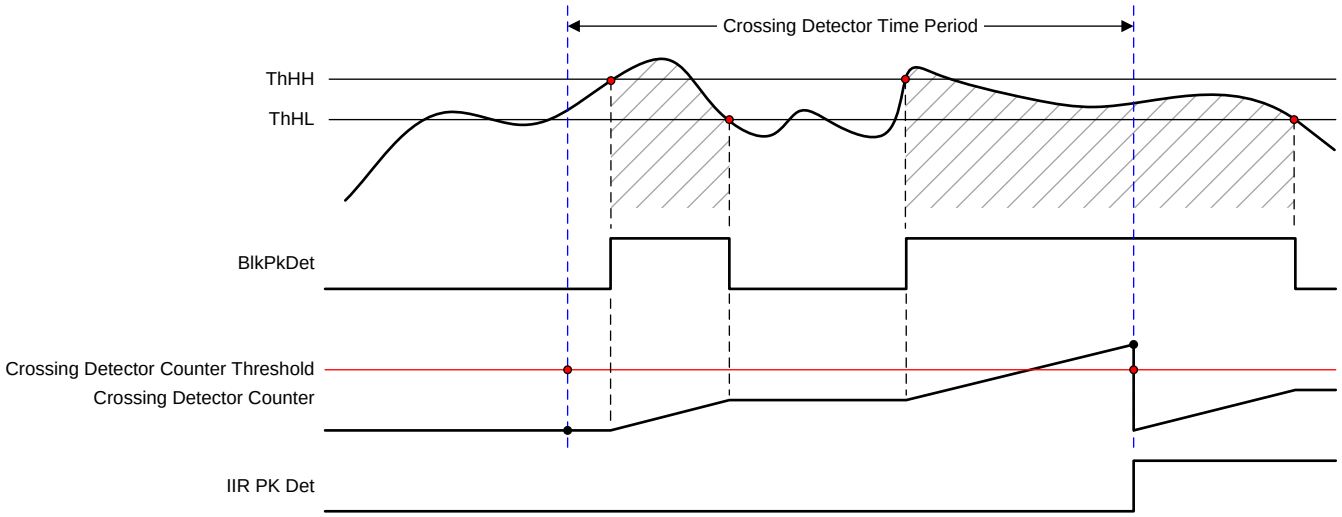

Figure 58. Crossing Detector Timing Diagram

Table 7 shows the register configurations required to set up the crossing detector. The detector operates in the f_S / 8 clock domain. The AGC modes may be configured separately for channel A (54xxh) and channel B (5Cxxh), although some registers are common in 54xxh (such as the GPIO pin selection).

Table 7. Registers Required for the Crossing Detector Operation

REGISTER	ADDRESS	DESCRIPTION
PKDET EN	5400h, 5C00h	Enables peak detector
BLKPKDET	5401h, 5402h, 5403h, 5C01h, 5C02h, 5C03h	Sets the block length N of number of samples (S`). Number of actual ADC samples is 8x this value: N is 17 bits: 1 to 2^{16}.
BLKTHHH, BLKTHHL, BLKTHLH, BLKTHLL	5407h, 5408h, 5409h, 540Ah, 5C07h, 5C08h, 5C09h, 5C0Ah	Sets the different thresholds for the hysteresis function values from 0 to 256 (where 256 is equivalent to the peak amplitude). For example: if BLKTHHH is to –2 dBFS from peak, $10^{(-2 / 20)} \times 256 = 203$, then set 5407h and 5C07h = CBh.
FILT0LPSEL	540Dh, 5C0Dh	Select block detector output or 2-bit output mode as the input to the interrupt identification register (IIR) filter.
TIMECONST	540Eh, 540Fh, 5C0Eh, 5C0Fh	Sets the crossing detector time period for N = 0 to 15 as 2N × f_S / 8 clock cycles. The maximum time period is 32768 × f_S / 8 clock cycles (approximately 87 µs at 3 GSPS).
FIL0THH, FIL0THL, FIL1THH, FIL1THL	540Fh-5412h, 5C0Fh-5C12h, 5416h-5419h, 5C16h-5C19h	Comparison thresholds for the crossing detector counter. These thresholds are 16-bit thresholds in 2.14-signed notation. A value of 1 (4000h) corresponds to 100% crossings, a value of 0.125 (0800h) corresponds to 12.5% crossings.
DWELLIIR	541Dh, 541Eh, 5C1Dh, 5C1Eh	DWELL counter for the IIR filter hysteresis.
IIR0 2BIT EN, IIR1 2BIT EN	5413h, 54114h, 5C13h, 5C114h	Enables 2-bit output format for the crossing detector.
OUTSEL GPIO[4:1]	5432h, 5433h, 5434h, 5435h	Connects the IIRPKDET0, IIRPKDET1 alarms to the GPIO pins; common register.
IODIR	5437h	Selects the direction for the four GPIO pins; common register.
RESET AGC	542Bh, 5C2Bh	After configuration, reset the AGC module to start operation.

8.3.8.3 RMS Power Detector

In this detector mode the peak power is computed for a block of N samples over a programmable block length and then compared against two sets of programmable thresholds (with hysteresis).

The RMS power detector circuit provides configuration options as shown in Figure 59. The RMS power value (1- or 2-bit) may be output onto the GPIO pins. In 2-bit output mode, two different thresholds are used whereas the 1-bit output provides one threshold together with hysteresis.

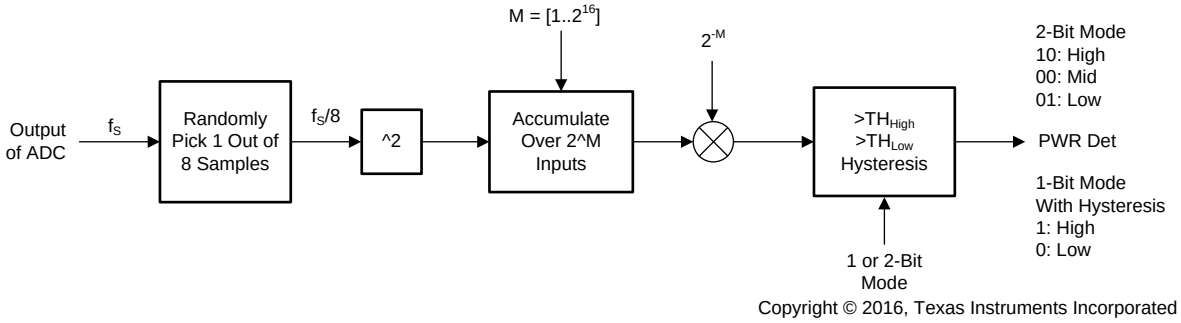

Figure 59. RMS Power Detector Implementation

Table 8 shows the register configurations required to set up the RMS power detector. The detector operates in the f_S / 8 clock domain. The AGC modes may be configured separately for channel A (54xxh) and channel B (5Cxxh), although some registers are common in 54xxh (such as the GPIO pin selection).

Table 8. Registers Required for Using the RMS Power Detector Feature

REGISTER	ADDRESS	DESCRIPTION
RMSDET EN	5420h, 5C20h	Enables RMS detector
PWRDETACCU	5421h, 5C21h	Programs the block length to be used for RMS power computation. The block length is defined in terms of f_S / 8 clocks. The block length may be programmed as 2^M with M = 0 to 16.
PWRDETH, PWRDETL	5422h, 5423h, 5424h, 5425h, 5C22h, 5C23h, 5C24h, 5C25h	The computed average power is compared against these high and low thresholds. One LSB of the thresholds represents 1 / 2^{16}. For example: is PWRDETH is set to –14 dBFS from peak, $[10^{(-14 / 20)}]^2 \times 2^{16}$ = 2609, then set 5422h, 5423h, 5C22h, 5C23h = 0A31h.
RMS2BIT EN	5427h, 5C27h	Enables 2-bit output format for the RMS detector output.
OUTSEL GPIO[4:1]	5432h, 5433h, 5434h, 5435h	Connects the PWRDET alarms to the GPIO pins; common register.
IODIR	5437h	Selects the direction for the four GPIO pins; common register.
RESET AGC	542Bh, 5C2Bh	After configuration, reset the AGC module to start operation.

8.3.8.4 GPIO AGC MUX

The GPIO pins may be used to control the NCO in wideband DDC mode or as alarm outputs for channel A and B. The GPIO pins may be configured through the SPI control to output the alarm from the peak power (1 bit), crossing detector (1 or 2 bit), faster overrange, or the RMS power output, as shown in Figure 60.

The programmable output MUX allows connecting any signal (including the NCO control) to any of the four GPIO pins. These pins may be configured as outputs (AGC alarm) or inputs (NCO control) through SPI programming.

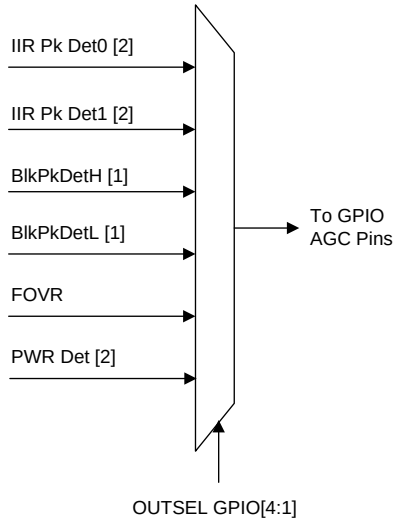

Figure 60. GPIO Output MUX Implementation

8.3.9 Power-Down Mode

The ADC32RF45 device provides a lot of configurability for the power-down mode. Power-down may be enabled using the PDN pin or the SPI register writes.

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8.3.10 ADC Test Pattern

The ADC32RF45 device provides several different options to output test patterns instead of the actual output data of the ADC in order to simplify the serial interface and system debug of the JESD204B digital interface link. The output data path is shown in Figure 61.

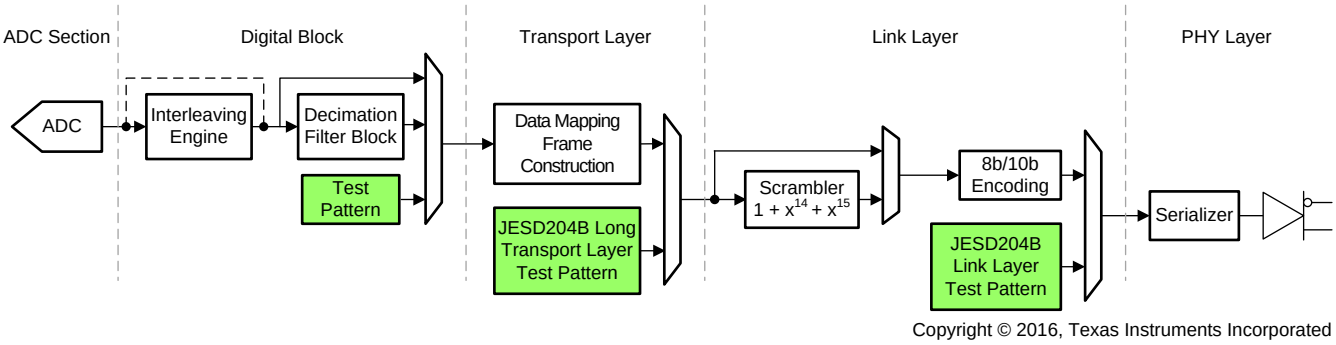

Figure 61. Test Pattern Generator Implementation

8.3.10.1 Digital Block

The ADC test pattern replaces the actual output data of the ADC. The test patterns shown in Table 9 are available in register 37h in the decimation filter page. When using the decimation filter, the test patterns are configured such that each converter (M) has a separate test pattern. The test patterns are synchronized for both ADC channels using the SYSREF signal.

NOTE

The number of converters increases in dual-band DDC mode and with a complex output.

Table 9. Test Pattern Options (Register 37h)

BIT	NAME	DEFAULT	DESCRIPTION
7-4	TEST PATTERN	0000	Test pattern outputs on channel A and B. 0000 = Normal operation using ADC output data 0001 = Outputs all 0s 0010 = Outputs all 1s 0011 = Outputs toggle pattern: output data are an alternating sequence of 10101010101010 and 01010101010101 0100 = Output digital ramp: output data increment by one LSB every clock cycle from code 0 to 16384 0110 = Single pattern: output data are a custom pattern 1 (75h and 76h) 0111 Double pattern: output data alternate between custom pattern 1 and custom pattern 2 1000 = Deskew pattern: output data are AAAAh 1001 = SYNC pattern: output data are FFFFh

8.3.10.2 Transport Layer

The transport layer maps the ADC output data into 8-bit octets and constructs the JESD204B frames using the LMFS parameters. Tail bits or 0's are added when needed. Alternatively, the JESD204B long transport layer test pattern may be substituted instead of the ADC data with the JESD frame, as shown in Table 10.

Table 10. Transport Layer Test Mode EN (Register 01h)

BIT	NAME	DEFAULT	DESCRIPTION
4	TESTMODE EN	0	Generates long transport layer test pattern mode according to section 5.1.6.3 of the JESD204B specification. 0 = Test mode disabled 1 = Test mode disabled

8.3.10.3 Link Layer

The link layer contains the scrambler and the 8b, 10b encoding of any data passed on from the transport layer. Additionally, the link layer also handles the initial lane alignment sequence that may be manually restarted.

The link layer test patterns are intended for testing the quality of the link (jitter testing and so forth). The test patterns do not pass through the 8b, 10b encoder and contain the options listed in Table 11.

Table 11. Link Layer Test Mode (Register 03h)

BIT	NAME	DEFAULT	DESCRIPTION
7-5	LINK LAYER TESTMODE	000	Generates a pattern according to section 5.3.3.8.2 of the JESD204B document. 000 = Normal ADC data 001 = D21.5 (high-frequency jitter pattern) 010 = K28.5 (mixed-frequency jitter pattern) 011 = Repeat the initial lane alignment (generates a K28.5 character and repeats lane alignment sequences continuously) 100 = 12-octet random pattern (RPAT) jitter pattern

Furthermore, a 2^{15} pseudorandom binary sequence (PRBS) may be enabled by setting up a custom test pattern (AAAAh) in the ADC section and running AAAAh through the 8b, 10b encoder with scrambling enabled.

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8.4 Device Functional Modes

8.4.1 Device Configuration

The ADC32RF45 device may be configured using a serial programming interface, as described in the *Serial Interface* section. In addition, the device has one dedicated parallel pin (PDN) for controlling the power-down modes.

8.4.2 Serial Interface

The ADC has a set of internal registers that may be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), and SDIN (serial interface data) pins. Serially shifting bits into the device is enabled when SEN is low. SDIN serial data are latched at every SCLK rising edge when SEN is active (low), as shown in Figure 62. The interface may function with SCLK frequencies from 5 MHz down to low speeds (of a few hertz) and also with a non-50% SCLK duty cycle, as shown in Table 12.

SPI access uses 24 bits consisting of eight register data bits, 12 register address bits, and four special bits to distinguish between read/write, page and register, and individual channel access, as described in Table 13.

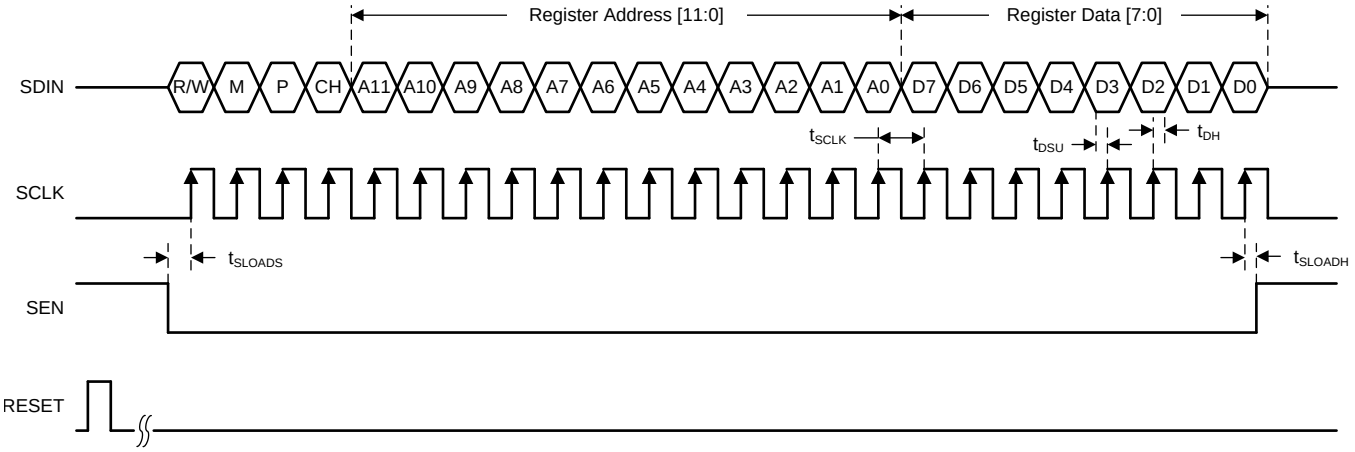

Figure 62. SPI Timing Diagram

Table 12. SPI Timing Information

		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to 1 / t_{SCLK})	1		5	MHz
t_{SLOADS}	SEN to SCLK setup time	50			ns
t_{SLOADH}	SCLK to SEN hold time	50			ns
t_{DSU}	SDIN setup time	50			ns
t_{DH}	SDIN hold time	0			ns

Table 13. SPI Input Description

SPI BIT	DESCRIPTION	OPTIONS
R/W bit	Read/write bit	0 = SPI write 1 = SPI read back
M bit	SPI bank access	0 = Analog SPI bank (master) 1 = All digital SPI banks (main digital, interleaving, decimation filter, JESD digital, and so forth)
P bit	JESD page selection bit	0 = Page access 1 = Register access
CH bit	SPI access for a specific channel of the JESD SPI bank	0 = Channel A 1 = Channel B
ADDR[11:0]	SPI address bits	—
DATA[7:0]	SPI data bits	—

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8.4.2.1 Serial Register Write: Analog Bank

The internal register of the ADC32RF45 analog SPI bank (Figure 63) may be programmed by:

1. Driving the SEN pin low.
2. Initiating a serial interface cycle specifying the page address of the register whose content must be written. Master page: write address 0012h with 04h.
3. Writing the register content. When a page is selected, multiple writes into the same page may be done.

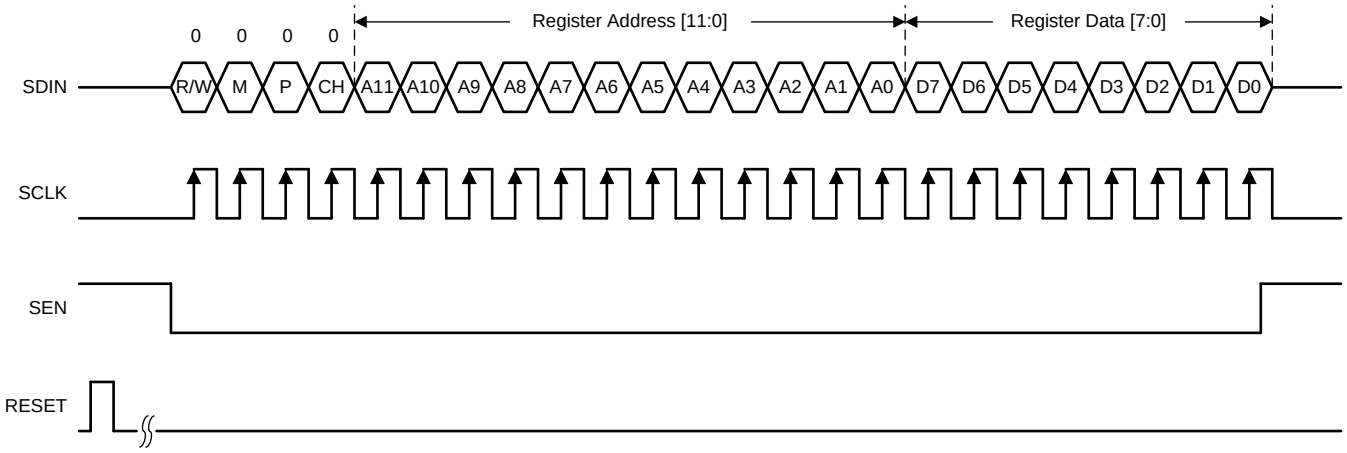

Figure 63. SPI Write Analog Bank Timing Diagram

8.4.2.2 Serial Register Readout: Analog Bank

Readback of the SPI content in one of the two analog banks (Figure 64) may be accomplished by:

1. Driving the SEN pin low.
2. Selecting the page address of the register whose content must be read. Master page: write address 0012h with 04h.
3. Setting the R/W bit to 1 and writing the address to be read back.
4. Reading back the register content on the SDOUT pin. When a page is selected, multiple read backs from the same page may be done.

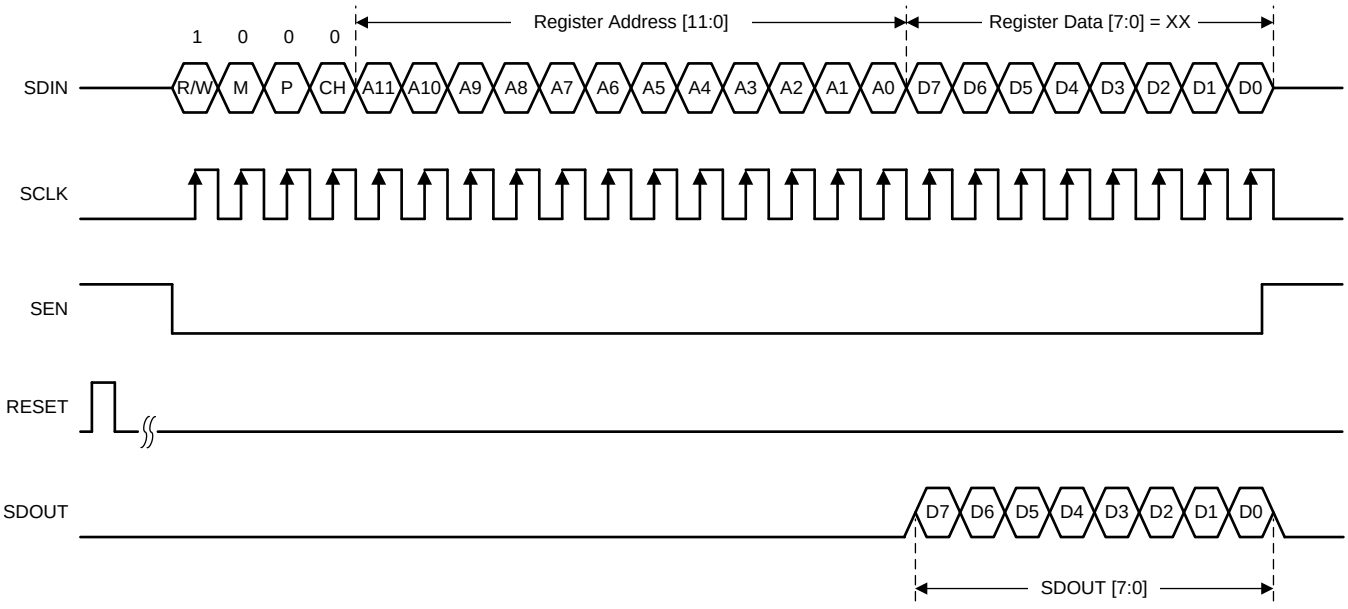

Figure 64. SPI Read Analog Bank Timing Diagram

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8.4.2.3 Digital Bank SPI Page Selection

The digital bank contains several pages (main digital, digital gain, and so forth). The timing for the individual page selection is shown in Figure 65. The individual pages may be selected by:

1. Driving the SEN pin low.
2. Setting the M bit to 1 and specifying the page with two register writes (note that the P bit must be set to 0).
   - Write address 4003h with 00h (LSB byte of the page address).
   - Write address 4004h (MSB byte of the page address).
   - Main digital page: write address 4004h with 68h.
   - JESD digital page: write address 4004h with 69h.
   - Digital gain page: write address 4004h with 61h and address 4002h with 05h.

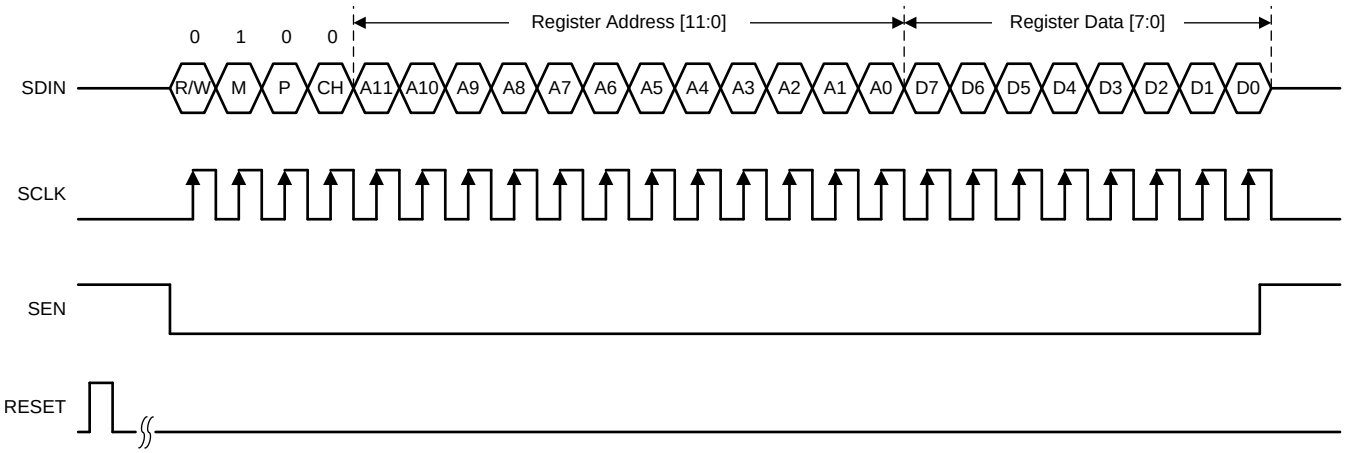

Figure 65. SPI Digital Bank Selection Timing Diagram

8.4.2.4 Serial Register Write: Digital Bank

The ADC32RF45 device is a dual-channel device and the JESD204B portion is configured individually for each channel using the CH bit after applying the sampling clock and SYSREF signal to the ADC. Note that the P bit must be set to 1 for register writes.

1. Drive the SEN pin low.
2. Select the JESD bank page (note that the M bit = 1 and the P bit = 0).
   - Write address 4003h with 00h.
   - Main digital page: write address 4004h with 68h.
   - JESD digital page: write address 4004h with 69h.
   - Digital gain page: write address 4004h with 61h and address 4002h with 05h.
3. Select the channel.
   - Main digital page: write address 4003h with 00h (channel A) or 01h (channel B).
   - JESD digital page: use the CH bit to select channel A (CH = 0) or channel B (CH = 1) and write the register content.
   - Digital gain page: write address 4003h with 00h (channel A) or 01h (channel B).

When a page is selected, multiple writes to the same page may be done.

8.4.2.5 Serial Register Readout: Digital Bank

Readback of the SPI content in one of digital banks (as shown in Figure 66) may be accomplished after applying the sampling clock and SYSREF signal to the ADC by:

1. Driving the SEN pin low.
2. Selecting the JESD bank page (note that the M bit = 1 and the P bit = 0).
   - Write address 4003h with 00h.
   - Main digital page: write address 4004h with 68h.
   - JESD digital page: write address 4004h with 69h.
   - Digital gain page: write address 4004h with 61h and address 4002h with 05h.
3. Set the R/W, M, and P bits to 1, select channel A or channel B, and write the address to be read back.
   - Main digital page: write address 4003h with 00h (channel A) or 01h (channel B).
   - Digital page: use the CH bit to select channel A (CH = 0) or channel B (CH = 1).
   - Digital gain page: write address 4003h with 00h (channel A) or 01h (channel B).
4. Read back the register content on the SDOUT pin. When a page is selected, multiple read backs from the same page may be done.

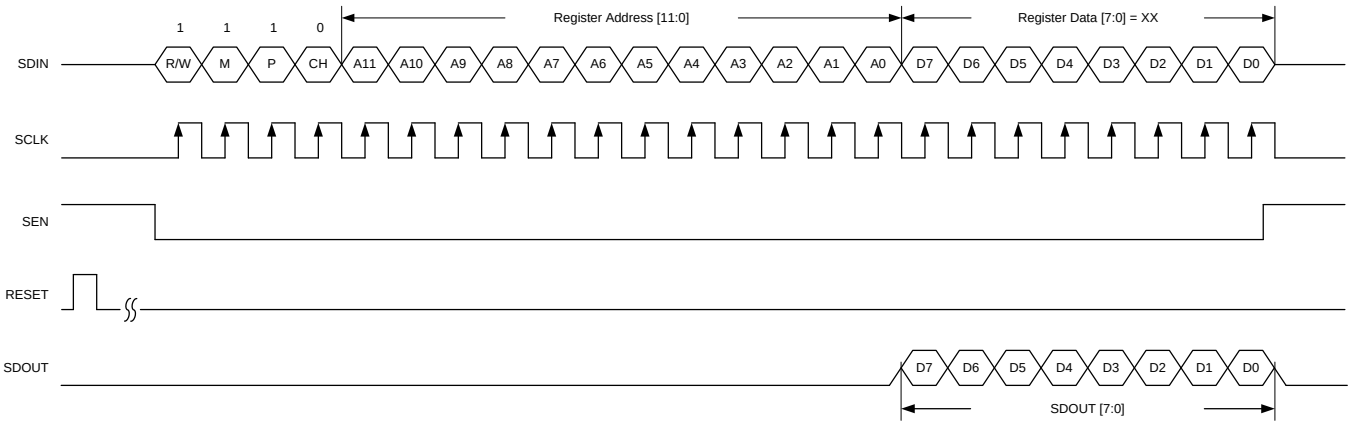

Figure 66. Serial Register Read Timing Diagram

8.4.2.6 Serial Register Write: Decimation Filter and Power Detector Pages

The decimation filter and power detector pages are special pages that accept direct addressing. The sampling clock and SYSREF signal are needed to properly configure the decimation settings. A timing diagram for this operation is shown in Figure 67.

1. Drive the SEN pin low.
2. Directly write to the decimation filter or power detector pages.
   - Decimation filter page: Write address 50xxh for channel A or 58xxh for channel B.
   - Power detector page: Write address 54xxh for channel A or 5Cxxh for channel B.

Example: 5001h addresses 01h in the decimation filter page for channel A.

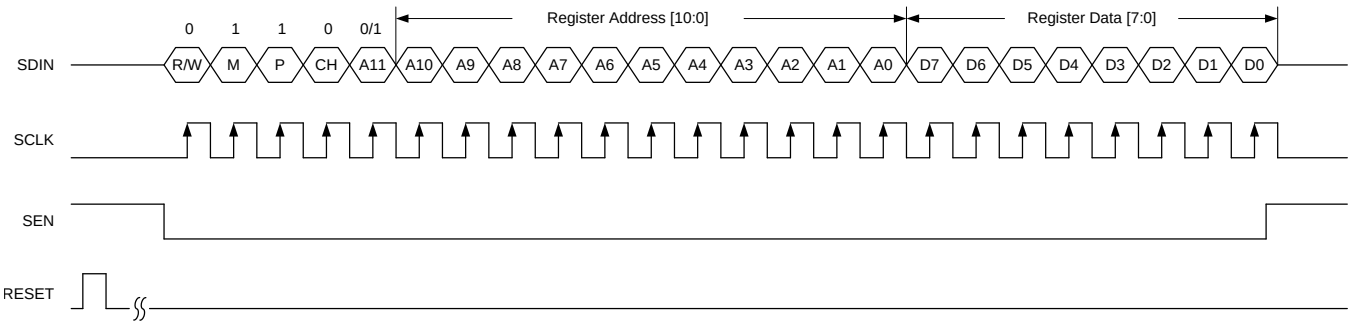

Figure 67. Serial Register Write Timing Diagram for Decimation Filter Page

8.4.3 JESD204B Interface

The ADC32RF45 device supports device subclass 1 with a maximum output data rate of 12.3 Gbps for each serial transmitter.

An external SYSREF signal is used to align all internal clock phases and the local multiframe clock to a specific sampling clock edge. This alignment allows synchronization of multiple devices in a system and minimizes timing and alignment uncertainty. The SYNCB input is used to control the JESD204B SerDes blocks, as shown in Figure 68.

Depending on the ADC sampling rate, the JESD204B output interface may be operated with one, two, or four lanes per ADC channel. The JESD204B setup and configuration of the frame assembly parameters is controlled through the SPI interface.

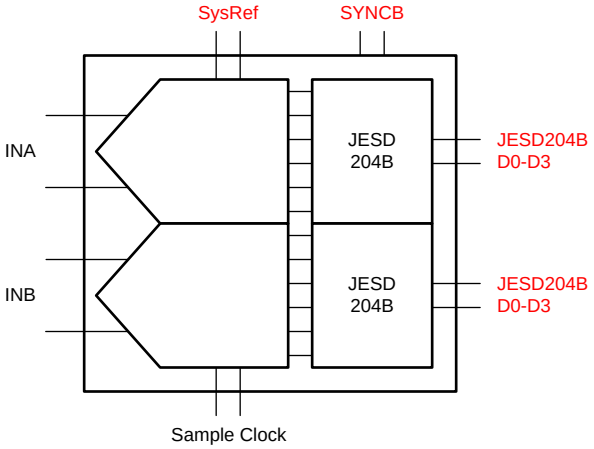

Figure 68. JESD Signal Overview

The JESD204B transmitter block consists of the transport layer, the data scrambler, and the link layer, as shown in Figure 69. The transport layer maps the ADC output data into the selected JESD204B frame data format and manages if the ADC output data or test patterns are transmitted. The link layer performs the 8b, 10b data encoding as well as the synchronization and initial lane alignment using the SYNC input signal. Optionally, data from the transport layer may be scrambled.

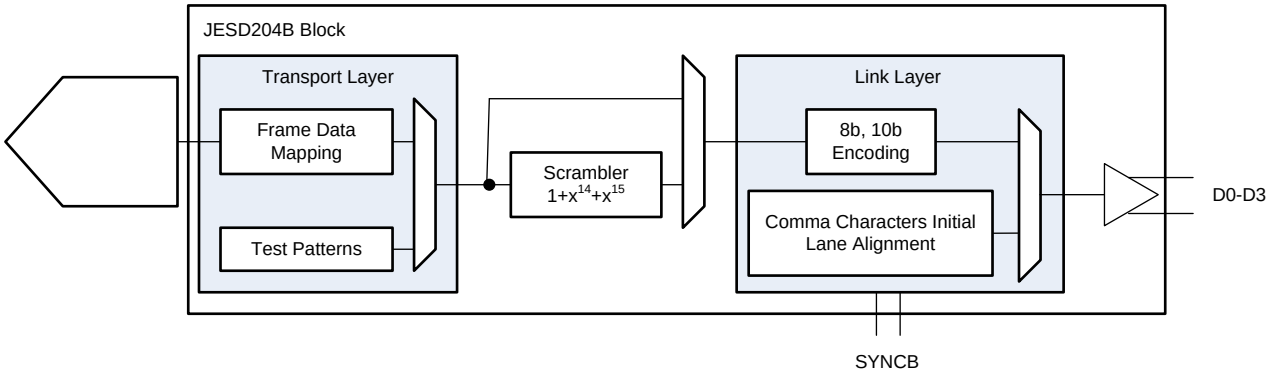

Figure 69. JESD Digital Block Implementation

8.4.3.1 JESD204B Initial Lane Alignment (ILA)

The receiving device starts the initial lane alignment process by deasserting the SYNCB signal. The SYNCB signal may be issued using the SYNCB input pins or by setting the proper SPI bits. When a logic low is detected on the SYNCB input, the ADC32RF45 device starts transmitting comma (K28.5) characters to establish the code group synchronization, as shown in Figure 70.

When synchronization completes, the receiving device reasserts the SYNCB signal and the ADC32RF45 device starts the initial lane alignment sequence with the next local multiframe clock boundary. The ADC32RF45 device transmits four multiframes, each containing K frames (K is SPI programmable). Each of the multiframes contains the frame start and end symbols. The second multiframe also contains the JESD204 link configuration data.

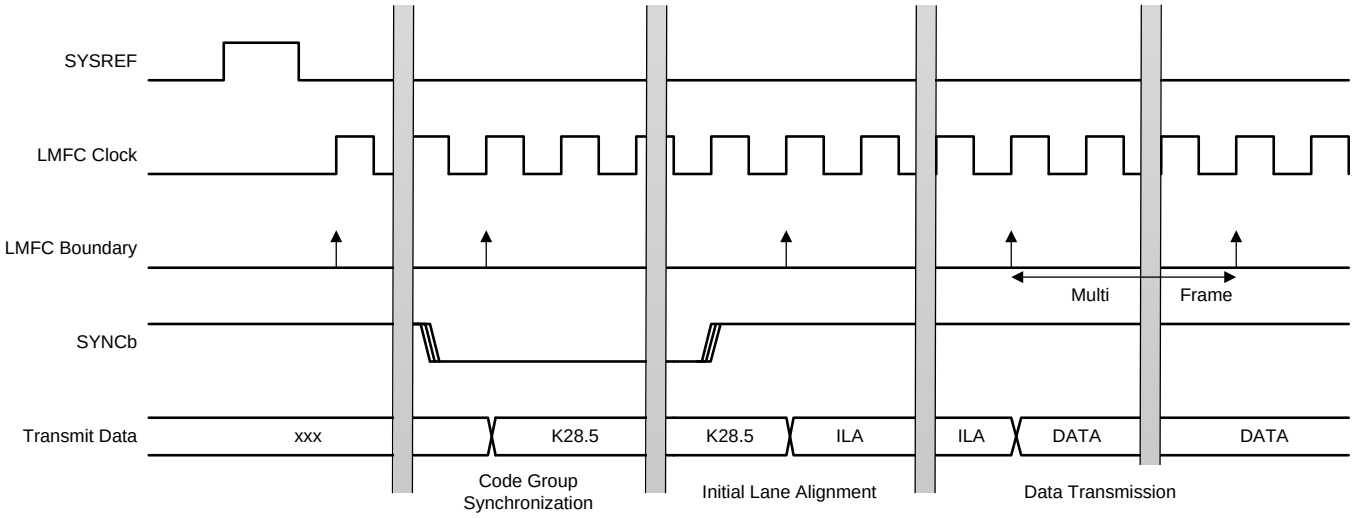

Figure 70. JESD Internal Timing Information

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8.4.3.2 JESD204B Frame Assembly

The JESD204B standard defines the following parameters:

- F is the number of octets per frame clock period
- L is the number of lanes per link
- M is the number of converters for the device
- S is the number of samples per frame

8.4.3.3 JESD204B Frame Assembly in Bypass Mode

Table 14 lists the available JESD204B formats and valid ranges for the ADC32RF45 device. The ranges are limited by the SerDes line rate and the maximum ADC sample frequency. The sample alignment for the bypass modes on the different lanes is shown in Table 15.

Table 14. JESD Mode Options: Bypass Mode

DECIMATION SETTING (Complex)	OUTPUT RESOLUTION (Bits)	L	M	F	S	12-BIT MODE	PLL MODE	JESD MODE 0	JESD MODE 1	JESD MODE 2	MAX f_{CLK} (Gsps)	RATIO [f_{SerDes} / f_{CLK} (Gbps / GSPS)]
Bypass	12 (1)	8	2	8	20	3	16x	3	0	0	3	4
	14	8	2	2	4	0	20x	1	0	0	2.46	5
	14	4	2	1	1	0	40x	0	1	0	1.23	10

(1) In full rate output, the two LSBs are truncated to a 12-bit output.

Table 15. JESD Sample Lane Alignments: Bypass Mode (1)

OUTPUT LANE	LMFS = 4211	LMFS = 8224		LMFS = 82820							
DA0		A_0[13:6]	A_0[5:0], 00	A_0[11:4]	A_0[3:0], A_1[11:8]	A_1[7:0]	A_2[11:4]	A_2[3:0], A_3[11:8]	A_3[7:0]	A_4[11:4]	A_4[3:0], 0000
DA1	A_0[13:6]	A_1[13:6]	A_1[5:0], 00	A_5[11:4]	A_5[3:0], A_6[11:8]	A_6[7:0]	A_7[11:4]	A_7[3:0], A_8[11:8]	A_8[7:0]	A_9[11:4]	A_9[3:0], 0000
DA2	A_0[5:0], 00	A_2[13:6]	A_2[5:0], 00	A_{10}[11:4]	A_{10}[3:0], A_{11}[11:8]	A_{11}[7:0]	A_{12}[11:4]	A_{12}[3:0], A_{13}[11:8]	A_{13}[7:0]	A_{14}[11:4]	A_{14}[3:0], 0000
DA3		A_3[13:6]	A_3[5:0], 00	A_{15}[11:4]	A_{15}[3:0], A_{16}[11:8]	A_{16}[7:0]	A_{17}[11:4]	A_{17}[3:0], A_{18}[11:8]	A_{18}[7:0]	A_{19}[11:4]	A_{19}[3:0], 0000
DB0		B_0[13:6]	B_0[5:0], 00	B_0[11:4]	B_0[3:0], B_1[11:8]	B_1[7:0]	B_2[11:4]	B_2[3:0], B_3[11:8]	B_3[7:0]	B_4[11:4]	B_4[3:0], 0000
DB1	B_0[13:6]	B_1[13:6]	B_1[5:0], 00	B_5[11:4]	B_5[3:0], B_6[11:8]	B_6[7:0]	B_7[11:4]	B_7[3:0], B_8[11:8]	B_8[7:0]	B_9[11:4]	B_9[3:0], 0000
DB2	B_0[5:0], 00	B_2[13:6]	B_2[5:0], 00	B_{10}[11:4]	B_{10}[3:0], B_{11}[11:8]	B_{11}[7:0]	B_{12}[11:4]	B_{12}[3:0], B_{13}[11:8]	B_{13}[7:0]	B_{14}[11:4]	B_{14}[3:0], 0000
DB3		B_3[13:6]	B_3[5:0], 00	B_{15}[11:4]	B_{15}[3:0], B_{16}[11:8]	B_{16}[7:0]	B_{17}[11:4]	B_{17}[3:0], B_{18}[11:8]	B_{18}[7:0]	B_{19}[11:4]	B_{19}[3:0], 0000

(1) Blue shading indicates channel A and yellow shading indicates channel B.

8.4.3.4 JESD204B Frame Assembly with Decimation (Single-Band DDC): Complex Output

Table 16 lists the available JESD204B interface formats and valid ranges for the ADC32RF45 device with decimation (single-band DDC) when using a complex output format. The ranges are limited by the SerDes line rate and the maximum ADC sample frequency. The sample alignment on the different lanes is shown in Table 17.

Table 16. JESD Mode Options: Single-Band Complex Output

DECIMATION SETTING (Complex)	NUMBER OF ACTIVE DDCS	L	M	F	S	PLL MODE	JESD MODE0	JESD MODE1	JESD MODE2	RATIO [f_{SerDes} / f_{CLK} (Gbps / GSPS)]
Divide-by-4	1 per channel	8	4	1	1	20x	1	1	0	2.5
		8	4	2	2	20x	1	0	0	
		4	4	2	1	40x	0	0	1	5
		4	4	4	2	40x	2	0	0	
Divide-by-6	1 per channel	8	4	1	1	20x	1	1	0	1.67
		8	4	2	2	20x	1	0	0	
		4	4	2	1	40x	0	0	1	3.33
		4	4	4	2	40x	2	0	0	
Divide-by-8	1 per channel	4	4	2	1	20x	1	0	0	2.5
		2	4	4	1	40x	2	0	0	5
Divide-by-9	1 per channel	4	4	2	1	20x	1	0	0	2.22
		2	4	4	1	40x	2	0	0	4.44
Divide-by-10	1 per channel	4	4	2	1	20x	1	0	0	2
		2	4	4	1	40x	2	0	0	4
Divide-by-12	1 per channel	4	4	2	1	20x	1	0	0	1.67
		2	4	4	1	40x	2	0	0	3.33
Divide-by-16	1 per channel	4	4	2	1	20x	1	0	0	1.25
		2	4	4	1	40x	2	0	0	2.5
Divide-by-18	1 per channel	4	4	2	1	20x	1	0	0	1.11
		2	4	4	1	40x	2	0	0	2.22
Divide-by-20	1 per channel	4	4	2	1	20x	1	0	0	1
		2	4	4	1	40x	2	0	0	2
Divide-by-24	1 per channel	4	4	2	1	20x	1	0	0	1.67
Divide-by-32	1 per channel	2	4	4	1	40x	2	0	0	1.25

Table 17. JESD Sample Lane Alignments: Single-Band Complex Output(1)

OUTPUT LANE	LMFS = 8411	LMFS = 8422		LMFS = 4421 20X		LMFS = 4421 40X		LMFS = 4442				LMFS = 2441			
DA0	AI_0 [15:8]	AI_0 [15:8]	AI_0 [7:0]	AI_0 [15:8]	AI_0 [7:0]										
DA1	AI_0 [7:0]	AI_1 [15:8]	AI_1 [7:0]	AQ_0 [15:8]	AQ_0 [7:0]	AI_0 [15:8]	AI_0 [7:0]	AI_0 [15:8]	AI_0 [7:0]	AI_1 [15:8]	AI_1 [7:0]	AI_0 [15:8]	AI_0 [7:0]	AQ_0 [15:8]	AQ_0 [7:0]
DA2	AQ_0 [15:8]	AQ_0 [15:8]	AQ_0 [7:0]			AQ_0 [15:8]	AQ_0 [7:0]	AQ_0 [15:8]	AQ_0 [7:0]	AQ_1 [15:8]	AQ_1 [7:0]				
DA3	AQ_0 [7:0]	AQ_1 [15:8]	AQ_1 [7:0]												
DB0	BI_0 [15:8]	BI_0 [15:8]	BI_0 [7:0]	BI_0 [15:8]	BI_0 [7:0]										
DB1	BI_0 [7:0]	BI_1 [15:8]	BI_1 [7:0]	BQ_0 [15:8]	BQ_0 [7:0]	BI_0 [15:8]	BI_0 [7:0]	BI_0 [15:8]	BI_0 [7:0]	BI_1 [15:8]	BI_1 [7:0]	BI_0 [15:8]	BI_0 [7:0]	BQ_0 [15:8]	BQ_0 [7:0]
DB2	BQ_0 [15:8]	BQ_0 [15:8	BQ_0 [7:0]			BQ_0 [15:8]	BQ_0 [7:0]	BQ_0 [15:8]	BQ_0 [7:0]	BQ_1 [15:8]	BQ_1 [7:0]				
DB3	BQ_0 [7:0]	BQ_1 [15:8]	BQ_1 [7:0]												

(1) Blue shading indicates channel A and yellow shading indicates channel B.

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8.4.3.5 JESD204B Frame Assembly with Decimation (Single-Band DDC): Real Output

Table 18 lists the available JESD204B formats and valid ranges for the ADC32RF45 device with decimation (single-band DDC) when using real output format. The ranges are limited by the SerDes line rate and the maximum ADC sample frequency. The sample alignment on the different lanes is shown in Table 19.

Table 18. JESD Mode Options: Single-Band Real Output (Wide Bandwidth)

DECIMATION SETTING (Complex)	NUMBER OF ACTIVE DDCS	L	M	F	S	PLL MODE	JESD MODE0	JESD MODE1	JESD MODE2	RATIO [f_{SerDes} / f_{CLK} (Gbps / GSPS)]
Divide-by-4 (Divide-by-2 real)	1 per channel	8	2	2	4	20x	1	0	0	2.5
		4	2	4	4	40x	2	0	0	5
		4	2	1	1	40x	0	0	1	
Divide-by-6 (Divide-by-3 real)	1 per channel	8	2	2	4	20x	1	0	0	1.67
		4	2	4	4	40x	2	0	0	3.33
		4	2	1	1	40x	0	0	1	

Table 19. JESD Sample Lane Alignment: Single-Band Real Output (Wide Bandwidth)(1)

OUTPUT LANE	LMFS = 8224		LMFS = 4244				LMFS = 4211
DA0	A_0[15:8]	A_0[7:0]					
DA1	A_1[15:8]	A_1[7:0]	A_0[15:8]	A_0[7:0]	A_1[15:8]	A_1[7:0]	A_0[15:8]
DA2	A_2[15:8]	A_2[7:0]	A_2[15:8]	A_2[7:0]	A_3[15:8]	A_3[7:0]	A_0[7:0]
DA3	A_3[15:8]	A_3[7:0]					
DB0	B_0[15:8]	B_0[7:0]					
DB1	B_1[15:8]	B_1[7:0]	B_0[15:8]	B_0[7:0]	B_1[15:8]	B_1[7:0]	B_0[15:8]
DB2	B_2[15:8]	B_2[7:0]	B_0[15:8]	B_2[7:0]	B_3[15:8]	B_3[7:0]	B_0[7:0]
DB3	B_3[15:8]	B_3[7:0]					

(1) Blue shading indicates channel A and yellow shading indicates channel B.

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8.4.3.6 JESD204B Frame Assembly with Decimation (Single-Band DDC): Real Output

Table 20 lists the available JESD204B formats and valid ranges for the ADC32RF45 device with decimation (dual-band DDC) when using a complex output format. The sample alignment on the different lanes is shown in Table 21.

Table 20. JESD Mode Options: Single-Band Real Output

DECIMATION SETTING (Complex)	NUMBER OF ACTIVE DDCS	L	M	F	S	PLL MODE	JESD MODE0	JESD MODE1	JESD MODE2	RATIO [f_{SerDes} / f_{CLK} (Gbps / GSPS)]
Divide-by-8 (Divide-by-4 real)	1 per channel	4	2	1	1	20x	1	1	0	2.5
		4	2	2	2	20x	1	0	0	
		2	2	2	1	40x	0	0	1	5
		2	2	4	2	40x	2	0	0	
Divide-by-9 (Divide-by-4.5 real)	1 per channel	4	2	1	1	20x	1	1	0	2.22
		4	2	2	2	20x	1	0	0	
		2	2	2	1	40x	0	0	1	4.44
		2	2	4	2	40x	2	0	0	
Divide-by-10 (Divide-by-5 real)	1 per channel	4	2	1	1	20x	1	1	0	2
		4	2	2	2	20x	1	0	0	
		2	2	2	1	40x	0	0	1	4
		2	2	4	2	40x	2	0	0	
Divide-by-12 (Divide-by-6 real)	1 per channel	4	2	1	1	20x	1	1	0	1.67
		4	2	2	2	20x	1	0	0	
		2	2	2	1	40x	0	0	1	3.33
		2	2	4	2	40x	2	0	0	
Divide-by-16 (Divide-by-8 real)	1 per channel	4	2	1	1	20x	1	1	0	1.25
		4	2	2	2	20x	1	0	0	
		2	2	2	1	40x	0	0	1	2.5
		2	2	4	2	40x	2	0	0	
Divide-by-18 (Divide-by-9 real)	1 per channel	4	2	1	1	20x	1	1	0	1.11
		4	2	2	2	20x	1	0	0	
		2	2	2	1	40x	0	0	1	2.22
		2	2	4	2	40x	2	0	0	
Divide-by-20 (Divide-by-10 real)	1 per channel	4	2	1	1	20x	1	1	0	1
		4	2	2	2	20x	1	0	0	
		2	2	2	1	40x	0	0	1	2
		2	2	4	2	40x	2	0	0	
Divide-by-24 (Divide-by-12 real)	1 per channel	2	2	2	1	40x	0	0	1	1.67
		2	2	4	2	40x	2	0	0	
Divide-by-32 (Divide-by-16 real)	1 per channel	2	2	2	1	40x	0	0	1	1.25
		2	2	4	2	40x	2	0	0	

Table 21. JESD Sample Lane Assignment: Single-Band Real Output(1)

OUTPUT LANE	LMFS = 4211	LMFS = 4222		LMFS = 2221		LMFS = 2242			
DA0	A_0[15:8]	A_0[15:8]	A_0[7:0]						
DA1	A_0[7:0]	A_1[15:8]	A_1[7:0]	A_0 [15:8]	A_0[7:0]	A_0[15:8]	A_0[7:0]	A_1[15:8]	A_1[7:0]
DB0	B_0[15:8]	B_0[15:8]	B_0[7:0]						
DB1	B_0[7:0]	B_1[15:8]	B_1[7:0]	B_0[15:8]	B_0[7:0]	B_0[15:8]	B_0[7:0]	B_1[15:8]	B_1[7:0]

(1) Blue shading indicates channel A and yellow shading indicates channel B.

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8.4.3.7 JESD204B Frame Assembly with Decimation (Dual-Band DDC): Complex Output

Table 22 lists the available JESD204B formats and valid ranges for the ADC32RF45 device with decimation (dual-band DDC) when using a complex output format. The ranges are limited by the SerDes line rate and the maximum ADC sample frequency. The sample alignment on the different lanes is shown in Table 23.

Table 22. JESD Mode Options: Dual-Band Complex Output

DECIMATION SETTING (Complex)	NUMBER OF ACTIVE DDCS	L	M	F	S	PLL MODE	JESD MODE0	JESD MODE1	JESD MODE2	RATIO [f_{SerDes} / f_{CLK} (Gbps / GSPS)]
Divide-by-8	2 per channel	8	8	2	1	20x	1	0	0	2.5
		4	8	4	1	40x	2	0	0	5
Divide-by-9	2 per channel	8	8	2	1	20x	1	0	0	2.22
		4	8	4	1	40x	2	0	0	4.44
Divide-by-10	2 per channel	8	8	2	1	20x	1	0	0	2
		4	8	4	1	40x	2	0	0	4
Divide-by-12	2 per channel	8	8	2	1	20x	1	0	0	1.67
		4	8	4	1	40x	2	0	0	3.33
Divide-by-16	2 per channel	8	8	2	1	20x	1	0	0	1.25
		4	8	4	1	40x	2	0	0	2.5
Divide-by-18	2 per channel	8	8	2	1	20x	1	0	0	1.11
		4	8	4	1	40x	2	0	0	2.22
Divide-by-20	2 per channel	8	8	2	1	20x	1	0	0	1
		4	8	4	1	40x	2	0	0	2
Divide-by-24	2 per channel	4	8	4	1	40x	2	0	0	1.67
Divide-by-32	2 per channel	4	8	4	1	40x	2	0	0	1.25

Table 23. JESD Sample Lane Assignment: Dual-Band Complex Output(1)

OUTPUT LANE	LMFS = 8821		LMFS = 4841			
DA0	$A1_0[15:8]$	$A1_0[7:0]$				
DA1	$A1Q_0[15:8]$	$A1Q_0[7:0]$	$A1I_0[15:8]$	$A1I_0[7:0]$	$A1Q_0[15:8]$	$A1Q_0[7:0]$
DA2	$A2I_0[15:8]$	$A2I_0[7:0]$	$A2I_0[15:8]$	$A2I_0[7:0]$	$A2Q_0[15:8]$	$A2Q_0[7:0]$
DA3	$A2Q_0[15:8]$	$A2Q_0[7:0]$				
DB0	$B1I_0[15:8]$	$B1I_0[7:0]$				
DB1	$B1Q_0[15:8]$	$B1Q_0[7:0]$	$B1I_0[15:8]$	$B1I_0[7:0]$	$B1Q_0[15:8]$	$B1Q_0[7:0]$
DB2	$B2I_0[15:8]$	$B2I_0[7:0]$	$B2I_0[15:8]$	$B2I_0[7:0]$	$B2Q_0[15:8]$	$B2Q_0[7:0]$
DB3	$B2Q_0[15:8]$	$B2Q_0[7:0]$				

(1) Blue and green shading indicates the two bands for channel A; yellow and orange shading indicates the two bands for channel B.

8.4.3.8 JESD204B Frame Assembly with Decimation (Dual-Band DDC): Real Output

Table 24 lists the available JESD204B formats and valid ranges for the ADC32RF45 device with decimation (dual-band DDC) when using real output format. The ranges are limited by the SerDes line rate and the maximum ADC sample frequency. The sample alignment on the different lanes is shown in Table 25.

Table 24. JESD Mode Options: Dual-Band Real Output

DECIMATION SETTING (Complex)	NUMBER OF ACTIVE DDCS	L	M	F	S	PLL MODE	JESD MODE0	JESD MODE1	JESD MODE2	RATIO [f_{SerDes} / f_{CLK} (Gbps / GSPS)]
Divide-by-8 (Divide-by-4 real)	2 per channel	8	4	1	1	20x	1	1	0	2.5
		8	4	2	2	20x	1	0	0	
		4	4	2	1	40x	0	0	1	5
		4	4	4	2	40x	2	0	0	
Divide-by-9 (Divide-by-4.5 real)	2 per channel	8	4	1	1	20x	1	1	0	2.22
		8	4	2	2	20x	1	0	0	
		4	4	2	1	40x	0	0	1	4.44
		4	4	4	2	40x	2	0	0	
Divide-by-10 (Divide-by-5 real)	2 per channel	8	4	1	1	20x	1	1	0	2
		8	4	2	2	20x	1	0	0	
		4	4	2	1	40x	0	0	1	4
		4	4	4	2	40x	2	0	0	
Divide-by-12 (Divide-by-6 real)	2 per channel	8	4	1	1	20x	1	1	0	1.67
		8	4	2	2	20x	1	0	0	
		4	4	2	1	40x	0	0	1	3.33
		4	4	4	2	40x	2	0	0	
Divide-by-16 (Divide-by-8 real)	2 per channel	8	4	1	1	20x	1	1	0	1.25
		8	4	2	2	20x	1	0	0	
		4	4	2	1	40x	0	0	1	2.5
		4	4	4	2	40x	2	0	0	
Divide-by-18 (Divide-by-9 real)	2 per channel	8	4	1	1	20x	1	1	0	1.11
		8	4	2	2	20x	1	0	0	
		4	4	2	1	40x	0	0	1	2.22
		4	4	4	2	40x	2	0	0	
Divide-by-20 (Divide-by-10 real)	2 per channel	8	4	1	1	20x	1	1	0	1
		8	4	2	2	20x	1	0	0	
		4	4	2	1	40x	0	0	1	2
		4	4	4	2	40x	2	0	0	
Divide-by-24 (Divide-by-12 real)	2 per channel	4	4	2	1	40x	0	0	1	1.67
		4	4	4	2	40x	2	0	0	
Divide-by-32 (Divide-by-16 real)	2 per channel	4	4	2	1	40x	0	0	1	1.25
		4	4	4	2	40x	2	0	0	

Table 25. JESD Sample Lane Assignment: Dual-Band Complex Output(1)

OUTPUT LANE	LMFS = 8411	LMFS = 8422		LMFS = 4421		LMFS = 4442			
DA0	$A1_0$[15:8]	$A1_0$[15:8]	$A1_0$[7:0]						
DA1	$A1_0$[7:0]	$A1_1$[15:8]	$A1_1$[7:0]	$A1_0$[15:8]	$A1_0$[7:0]	$A1_0$[15:8]	$A1_0$[7:0]	$A1_1$[15:8]	$A1_1$[7:0]
DA2	$A2_0$[15:8]	$A2_0$[15:8]	$A2_0$[7:0]	$A2_0$[15:8]	$A2_0$[7:0]	$A2_0$[15:8]	$A2_0$[7:0]	$A2_1$[15:8]	$A2_1$[7:0]
DA3	$A2_0$[7:0]	$A2_1$[15:8]	$A2_1$[7:0]						
DB0	$B1_0$[15:8]	$B1_0$[15:8]	$B1_0$[7:0]						
DB1	$B1_0$[7:0]	$B1_1$[15:8]	$B1_1$[7:0]	$B1_0$[15:8]	$B1_0$[7:0]	$B1_0$[15:8]	$B1_0$[7:0]	$B1_1$[15:8]	$B1_1$[7:0]
DB2	$B2_0$[15:8]	$B2_0$[15:8]	$B2_0$[7:0]	$B2_0$[15:8]	$B2_0$[7:0]	$B2_0$[15:8]	$B2_0$[7:0]	$B2_1$[15:8]	$B2_1$[7:0]
DB3	$B2_0$[7:0]	$B2_1$[15:8]	$B2_1$[7:0]						

(1) Blue and green shading indicates the two bands for channel A; yellow and orange shading indicates the two bands for channel B.

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8.5 Register Maps

The ADC32RF45 device contains two main SPI banks. The analog SPI bank provides access to the ADC core and the digital SPI bank controls the digital blocks (including the serial JESD interface). The analog SPI bank contains the master and ADC pages. The digital SPI bank is divided into multiple pages (the main digital, digital gain, decimation filter, JESD digital, and power detector pages). Table 26 lists a register map for the ADC32RF45 device.

Table 26. Register Map

REGISTER ADDRESS A[11:0] (Hex)	REGISTER DATA							
	7	6	5	4	3	2	1	0
GENERAL REGISTERS								
000	RESET	0	0	0	0	0	0	RESET
011	ADC PAGE SEL							
012	0	0	0	0	0	MASTER PAGE SEL	0	0
MASTER PAGE (M = 0)								
020	0	0	0	PDN SYSREF	0	PDN CHA	PDN CHB	GLOBAL PDN
025, 026, 027, 029, 02A, 02C, 02D, 02F, 034	See Table 102 for more details							
039	0	1	0	1	0	PDN CHA EN	PDN CHB EN	SYNC TERM DIS
03B	See Table 102 for more details							
03C	0	SYSREF DEL EN	0	0	0	0	SYSREF DEL[4:3]	
03D	0	0	0	0	0	JESD OUTPUT SWING		
03F, 040, 042, 043, 045, 046, 048, 049, 04B, 053, 059	See Table 102 for more details							
05A	SYSREF DEL[2:0]			0	0	0	0	0
05B, 05C	See Table 102 for more details							
058	0	0	SYNCB POL	0	0	0	0	0
062, 065, 06B, 06C, 06E, 06F, 070, 071, 076, 077, 07D, 081, 084, 08A, 08E	See Table 102 for more details							

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Register Maps (continued)

Table 26. Register Map (continued)

REGISTER ADDRESS A[11:0] (Hex)	REGISTER DATA							
	7	6	5	4	3	2	1	0
ADC PAGE (FFh, M = 0)								
022, 032, 033, 042, 043, 045, 046, 047, 053, 054, 05C, 064, 072, 083, 08C, 097	See Table 102 for more details							
0D5	0	0	0	0	0	SLOW SP EN1	0	0
0D8	0	0	0	SLOW SP EN2	0	0	0	0
0F0, 0F1	See Table 102 for more details							
DIGITAL GAIN PAGE (610005h, M = 1 for Channel A and 610105h, M = 1 for Channel B)								
0A6	0	0	0	0	DIG GAIN			
MAIN DIGITAL PAGE (6800h, M = 1)								
000	0	0	0	0	0	0	0	DIG RESET
044	0	0	LOOP EN1	0	0	0	0	0
068	0	LOOP EN2	0	0	0	0	0	0
0A2	0	0	0	0	NQ ZONE EN	NYQUIST ZONE		
JESD DIGITAL PAGE (6900h, M = 1)								
001	CTRL K	0	0	TESTMODE EN	0	LANE ALIGN	FRAME ALIGN	TX LINK DIS
002	SYNC REG	SYNC REG EN	0	0	12BIT MODE		JESD MODE0	
003	LINK LAYER TESTMODE			LINK LAY RPAT	LMFC MASK RES	JESD MODE1	JESD MODE2	RAMP 12BIT
004	0	0	0	0	0	0	REL ILA SEQ	
006	SCRAMBLE EN	0	0	0	0	0	0	0
007	0	0	0	FRAMES PER MULTIFRAME (K)				
016	0	40X MODE			0	0	0	0
017	0	0	0	0	LANE0 POL	LANE1 POL	LANE2 POL	LANE3 POL
032	SEL EMP LANE 0						0	0
033	SEL EMP LANE 1						0	0
034	SEL EMP LANE 2						0	0
035	SEL EMP LANE 3						0	0
036	0	CMOS SYNCB	0	0	0	0	0	0
037	0	0	0	0	0	0	PLL MODE	

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Register Maps (continued)

Table 26. Register Map (continued)

REGISTER ADDRESS A[11:0] (Hex)	REGISTER DATA							
	7	6	5	4	3	2	1	0
DECIMATION FILTER PAGE (Direct Addressing, 16-Bit Address, 5000h for Channel A and 5800h for Channel B)								
000	0	0	0	0	0	0	0	DDC EN
001	0	0	0	0	DECIM FACTOR			
002	0	0	0	0	0	0	0	DUAL BAND EN
005	0	0	0	0	0	0	0	REAL OUT EN
006	0	0	0	0	0	0	0	DDC MUX
007	DDC0 NCO1 LSB							
008	DDC0 NCO1 MSB							
009	DDC0 NCO2 LSB							
00A	DDC0 NCO2 MSB							
00B	DDC0 NCO3 LSB							
00C	DDC0 NCO3 MSB							
00D	DDC1 NCO4 LSB							
00E	DDC1 NCO4 MSB							
00F	0	0	0	0	0	0	0	NCO SEL PIN
010	0	0	0	0	0	0	NCO SEL	
011	0	0	0	0	0	0	LMFC RESET MODE	
014	0	0	0	0	0	0	0	DDC0 6DB GAIN
016	0	0	0	0	0	0	0	DDC1 6DB GAIN
01E	0	DDC DET LAT			0	0	0	0
01F	0	0	0	0	0	0	0	WBF 6DB GAIN
033	TEST PATTERN1[7:0]							
034	TEST PATTERN1[15:8]							
035	TEST PATTERN2[7:0]							
036	TEST PATTERN2[15:8]							
037	0	0	0	0	TEST PATTERN SEL			
03A	0	0	0	0	0	0	TEST PAT RES	TP RES EN

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Register Maps (continued)

Table 26. Register Map (continued)

REGISTER ADDRESS A[11:0] (Hex)	REGISTER DATA							
	7	6	5	4	3	2	1	0
POWER DETECTOR PAGE (Direct Addressing, 16-Bit Address, 5400h for Channel A and 5C00h for Channel B)								
000	0	0	0	0	0	0	0	PKDET EN
001	BLKPKDET [7:0]							
002	BLKPKDET [15:8]							
003	0	0	0	0	0	0	0	BLKPKDET [16]
007	BLKTHHH							
008	BLKTHHL							
009	BLKTHLH							
00A	BLKTHLL							
00B	DWELL[7:0]							
00C	DWELL[15:8]							
00D	0	0	0	0	0	0	0	FILT0LPSEL
00E	0	0	0	0	TIMECONST			
00F	FIL0THH[7:0]							
010	FIL0THH[15:8]							
011	FIL0THL[7:0]							
012	FIL0THL[15:8]							
013	0	0	0	0	0	0	0	IIR0 2BIT EN
016	FIL1THH[7:0]							
017	FIL1THH[15:8]							
018	FIL1THL[7:0]							
019	FIL1THL[15:8]							
01A	0	0	0	0	0	0	0	IIR1 2BIT EN
01D	DWELLIIR[7:0]							
01E	DWELLIIR[15:8]							
020	0	0	0	0	0	0	0	IIR0 2BIT EN
021	0	0	0	PWRDETACCU				
022	PWRDETH[7:0]							
023	PWRDETH[15:8]							
024	PWRDETL[7:0]							
025	PWRDETL[15:8]							

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Register Maps (continued)

Table 26. Register Map (continued)

REGISTER ADDRESS A[11:0] (Hex)	REGISTER DATA							
	7	6	5	4	3	2	1	0
POWER DETECTOR PAGE (continued)								
027	0	0	0	0	0	0	0	RMS 2BIT EN
02B	0	0	0	RESET AGC	0	0	0	0
032	OUTSEL GPIO1							
033	OUTSEL GPIO2							
034	OUTSEL GPIO3							
035	OUTSEL GPIO4							
037	0	0	0	0	IODIR GPIO4	IODIR GPIO3	IODIR GPIO2	IODIR GPIO1
038	0	0	INSEL1		0	0	INSEL0	

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8.5.1 Example Register Writes

This section provides three different example register writes. Table 27 describes a global power-down register write, Table 28 describes the register writes when the scrambler is enabled, and Table 29 describes the register writes for 8x decimation for channels A and B (complex output, 1 DDC mode) with the NCO set to 1.8 GHz (f_S = 3 GSPS) and the JESD format configured to LMFS = 4421.

Table 27. Global Power-Down

ADDRESS	DATA	COMMENT
12h	04h	Set the master page
20h	01h	Set the global power-down

Table 28. Scrambler Enable

ADDRESS	DATA	COMMENT
4004h	69h	Select the digital JESD page
4003h	00h	
6006h	80h	Scrambler enable, channel A
7006h	80h	Scrambler enable, channel B

Table 29. 8x Decimation for Channel A and B

ADDRESS	DATA	COMMENT
4004h	68h	Select the main digital page for channel A
4003h	00h	
6000h	01h	Issue a digital reset for channel A
6000h	00h	Clear the digital for reset channel A
4003h	01h	Select the main digital page for channel B
6000h	01h	Issue a digital reset for channel B
6000h	00h	Clear the digital reset for channel B
4004h	69h	Select the digital JESD page
4003h	00h	
6002h	01h	Set JESD MODE0 = 1, channel A
7002h	01h	Set JESD MODE0 = 1, channel B
5000h	01h	Enable DDC, channel A
5001h	02h	Set decimation to 8x complex
5007h	9Ah	Set the LSB of DDC0, NCO1 to 9Ah (f_{NCO} = 1.8 GHz, f_S = 3 GSPS)
5008h	99h	Set the MSB of DDC0, NCO1 to 99h (f_{NCO} = 1.8 GHz, f_S = 3 GSPS)
5014h	01h	Enable the 6-dB digital gain of DDC0
5801h	02h	Set decimation to 8x complex
5807h	9Ah	Set LSB of DDC0, NCO1 to 9Ah (f_{NCO} = 1.8 GHz, f_S = 3 GSPS)
5808h	99h	Set MSB of DDC0, NCO1 to 99h (f_{NCO} = 1.8 GHz, f_S = 3 GSPS)
5814h	01h	Enable the 6-dB digital gain of DDC0

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8.5.2 Register Descriptions

8.5.2.1 General Registers

8.5.2.1.1 Register 000h (address = 000h), General Registers

Figure 71. Register 000h

7	6	5	4	3	2	1	0
RESET	0	0	0	0	0	0	RESET
R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 30. Register 000h Field Descriptions

Bit	Field	Type	Reset	Description
7	RESET	R/W	0h	0 = Normal operation 1 = Internal software reset, clears back to 0
6-1	0	W	0h	Must write 0
0	RESET	R/W	0h	0 = Normal operation(1) 1 = Internal software reset, clears back to 0

(1) Both bits (7, 0) must be set simultaneously to perform a reset.

8.5.2.1.2 Register 011h (address = 011h), General Registers

Figure 72. Register 011h

7	6	5	4	3	2	1	0
ADC PAGE SEL							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 31. Register 011h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ADC PAGE SEL	R/W	0h	00000000 = Normal operation, ADC page is not selected 11111111 = ADC page is selected; MASTER PAGE SEL must be set to 0

8.5.2.1.3 Register 012h (address = 012h), General Registers

Figure 73. Register 012h

7	6	5	4	3	2	1	0
0	0	0	0	0	MASTER PAGE SEL	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 32. Register 012h Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0	W	0h	Must write 0
2	MASTER PAGE SEL	R/W	0h	0 = Normal operation 1 = Selects the master page address; ADC PAGE must be set to 0
1-0	0	W	0h	Must write 0

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8.5.3 Master Page (M = 0)

8.5.3.1 Register 020h (address = 020h), Master Page

Figure 74. Register 020h

7	6	5	4	3	2	1	0
0	0	0	PDN SYSREF	0	PDN CHA	PDN CHB	GLOBAL PDN
W-0h	W-0h	W-0h	R/W-0h	W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 33. Register 020h Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	W	0h	Must write 0
4	PDN SYSREF	R/W	0h	This bit powers down the SYSREF input buffer. 0 = Normal operation 1 = SYSREF input capture buffer is powered down and further SYSREF input pulses are ignored
3	0	W	0h	Must write 0
2	PDN CHA	R/W	0h	This bit powers down channel A. 0 = Normal operation 1 = Channel A is powered down
1	PDN CHB	R/W	0h	This bit powers down channel B. 0 = Normal operation 1 = Channel B is powered down
0	GLOBAL PDN	R/W	0h	This bit enables the global power-down. 0 = Normal operation 1 = Global power-down enabled

8.5.3.2 Register 03Ch (address = 03Ch), Master Page

Figure 75. Register 03Ch

7	6	5	4	3	2	1	0
0	SYSREF DEL EN	0	0	0	0	SYSREF DEL[4:3]	
W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 34. Register 03Ch Field Descriptions

Bit	Field	Type	Reset	Description
7	0	W	0h	Must write 0
6	SYSREF DEL EN	R/W	0h	This bit allows an internal delay to be added to the SYSREF input. 0 = SYSREF delay disabled 1 = SYSREF delay enabled through register settings [3Ch (bits 1-0), 5Ah (bits 7-5)]
5-2	0	W	0h	Must write 0
1-0	SYSREF DEL[4:3]	R/W	0h	When the SYSREF delay feature is enabled (3Ch, bit 6) the delay may be adjusted in 25-ps steps; the first step is 175 ps. The PVT variation of each 25-ps step is ±10 ps. The 175-ps step is ±50 ps; see Table 36.

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8.5.3.3 Register 05Ah (address = 05Ah), Master Page

Figure 76. Register 05Ah

7	6	5	4	3	2	1	0
SYSREF DEL[2:0]			0	0	0	0	0
W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 35. Register 05Ah Field Descriptions

Bit	Field	Type	Reset	Description
7	SYSREF DEL2	W	0h	When the SYSREF delay feature is enabled (3Ch, bit 6) the delay may be adjusted in 25-ps steps; the first step is 175 ps. The PVT variation of each 25-ps step is ±10 ps. The 175-ps step is ±50 ps; see Table 36.
6	SYSREF DEL1	R/W		
5	SYSREF DEL0	W		
4-0	0	W	0h	Must write 0

Table 36. SYSREF DEL[2:0] Bit Settings

STEP	SETTING	STEP (NOM)	TOTAL DELAY (NOM)
1	01000	175 ps	175 ps
2	00111	25 ps	200 ps
3	00110	25 ps	225 ps
4	00101	25 ps	250 ps
5	00100	25 ps	275 ps
6	00011	25 ps	300 ps
7	00010	25 ps	TBD
8	00001	25 ps	TBD
9	00000	25 ps	TBD
10	11111	25 ps	TBD
11	11110	25 ps	TBD
…	…	…	…
25	10000	25 ps	TBD

8.5.3.4 Register 03Dh (address = 3Dh), Master Page

Figure 77. Register 03Dh

7	6	5	4	3	2	1	0
0	0	0	0	0	JESD OUTPUT SWING		
W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h		

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 37. Register 03Dh Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0	W	0h	Must write 0
2-0	JESD OUTPUT SWING	R/W	0h	These bits select the output amplitude, V_{OD} (mV_{PP}), of the JESD transmitter for all lanes. 0 = 860 mV_{PP} 1= 810 mV_{PP} 2 = 770 mV_{PP} 3 = 745 mV_{PP} 4 = 960 mV_{PP} 5 = 930 mV_{PP} 6 = 905 mV_{PP} 7 = 880 mV_{PP}

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8.5.3.5 Register 039h (address = 039h), Master Page

Figure 78. Register 039h

7	6	5	4	3	2	1	0
0	1	0	1	0	PDN CHA EN	PDN CHB EN	SYNC TERM DIS
W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 38. Register 039h Field Descriptions

Bit	Field	Type	Reset	Description
7	0	W	0h	Must write 0
6	1	W	0h	TBD
5	0	W	0h	Must write 0
4	1	W	0h	TBD
3	0	W	0h	Must write 0
2	PDN CHA EN	R/W	0h	This bit enables the power-down control of channel A through SPI in register 20h. 0 = PDN control disabled 1 = PDN control enabled
1	PDN CHB EN	R/W	0h	This bit enables the power-down control of channel B through SPI in register 20h. 0 = PDN control disabled 1 = PDN control enabled
0	SYNC TERM DIS	R/W	0h	This bit disables the on-chip, 100-Ω termination resistors on the SYNCB input. 0 = On-chip, 100-Ω termination enabled 1 = On-chip, 100-Ω termination disabled

8.5.3.6 Register 058h (address = 058h), Master Page

Figure 79. Register 058h

7	6	5	4	3	2	1	0
0	0	SYNCB POL	0	0	0	0	0
W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 39. Register 058h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0
5	SYNCB POL	R/W	0h	This bit inverts the SYNCB polarity. 0 = Polarity is not inverted; this setting matches the timing diagrams in this document and is the proper setting to use 1 = Polarity is inverted
4-0	0	W	0h	Must write 0

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8.5.4 ADC Page (FFh, M = 0)

8.5.4.1 Register 0D5h (address = 0D5h), ADC Page

Figure 80. Register 0D5h

7	6	5	4	3	2	1	0
0	0	0	0	0	SLOW SP EN1	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 40. Register 0D5h Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0	W	0h	Must write 0
2	SLOW SP EN1	R/W	0h	This bit must be enabled for clock rates below 1.75 GSPS. 0 = ADC sampling rates are faster than 1.75 GSPS 1 = ADC sampling rates are slower than 1.75 GSPS
1-0	0	W	0h	Must write 0

8.5.4.2 Register 0D8h (address = 0D8h), ADC Page

Figure 81. Register 0D8h

7	6	5	4	3	2	1	0
0	0	0	SLOW SP EN2	0	0	0	0
W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 41. Register 0D8h Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	W	0h	Must write 0
4	SLOW SP EN2	R/W	0h	This bit must be enabled for clock rates below 1.75 GSPS. 0 = ADC sampling rates are faster than 1.75 GSPS 1 = ADC sampling rates are slower than 1.75 GSPS
3-0	0	W	0h	Must write 0

8.5.5 Digital Gain Page (610005h, M = 1 for Channel A; 610105h, M = 1 for Channel B)

8.5.5.1 Register A6h (address = 0A6h), Digital Gain Page

Figure 82. Register 0A6h

7	6	5	4	3	2	1	0
0	0	0	0	DIG GAIN			
W-0h	W-0h	W-0h	W-0h	R/W-0h			

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 42. Register 0A6h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0
3-0	DIG GAIN	R/W	0h	These bits set the digital gain of the ADC output data prior to decimation up to 11 dB; see Table 43.

Table 43. DIG GAIN Bit Settings

SETTING	DIGITAL GAIN
0000	0 dB
0001	1 dB
0010	2 dB
…	…
1010	10 dB
1011	11 dB

8.5.6 Main Digital Page (6800h, M = 1)

8.5.6.1 Register 000h (address = 000h), Main Digital Page

Figure 83. Register 000h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DIG RESET
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 44. Register 000h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	DIG RESET	R/W	0h	This bit resets the digital core but does not self-clear and thus must be pulsed. 0 = Normal operation 1 = Software reset

8.5.6.2 Register 044h (address = 044h), Main Digital Page

Figure 84. Register 044h

7	6	5	4	3	2	1	0
0	0	LOOP EN1	0	0	0	0	0
W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 45. Register 044h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0
5	LOOP EN1	R/W	0h	This bit enables the analog loop interleaving correction. This bit must be enabled with LOOP EN2 in register 68h. The analog correction loop functions with the Nyquist zone information (A2h). 0 = Analog loop correction disabled 1 = Analog loop correction enabled
4-0	0	W	0h	Must write 0

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8.5.6.3 Register 068h (address = 068h), Main Digital Page

Figure 85. Register 068h

7	6	5	4	3	2	1	0
0	LOOP EN2	0	0	0	0	0	0
W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 46. Register 068h Field Descriptions

Bit	Field	Type	Reset	Description
7	0	W	0h	Must write 0
6	LOOP EN2	R/W	0h	This bit enables the analog loop interleaving correction. This bit must be enabled with LOOP EN1 in register 44h. The analog correction loop functions with the Nyquist zone information (A2h). 0 = Analog loop correction disabled 1 = Analog loop correction enabled
5-0	0	W	0h	Must write 0

8.5.6.4 Register 0A2h (address = 0A2h), Main Digital Page

Figure 86. Register 0A2h

7	6	5	4	3	2	1	0
0	0	0	0	NQ ZONE EN	NYQUIST ZONE		
W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h		

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 47. Register 0A2h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0
3	NQ ZONE EN	R/W	0h	This bit allows the Nyquist zone to be programmed for the analog correction loop. LOOP EN1, LOOP EN2 must be set to enable this correction feature. 0 = Nyquist zone specification disabled 1 = Nyquist zone specification enabled
2-0	NYQUIST ZONE	R/W	0h	These bits specify the operating Nyquist zone for the analog correction loop. 000 = 1st Nyquist zone (dc – f_S / 2) 001 = 2nd Nyquist zone (f_S / 2 – f_S) 010 = 3rd Nyquist zone 011 = 4th Nyquist zone 111 = For signals spanning multiple Nyquist zones

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8.5.7 JESD Digital Page (6900h, M = 1)

8.5.7.1 Register 001h (address = 001h), JESD Digital Page

Figure 87. Register 001h

7	6	5	4	3	2	1	0
CTRL K	0	0	TESTMODE EN	0	LANE ALIGN	FRAME ALIGN	TX LINK DIS
R/W-0h	W-0h	W-0h	R/W-0h	W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 48. Register 001h Field Descriptions

Bit	Field	Type	Reset	Description
7	CTRL K	R/W	0h	Enable bit for the number of frames per multiframe. 0 = Default is five frames per multiframe 1 = Frames per multiframe may be set in register 06h
6-5	0	R/W	0h	Must write 0
4	TESTMODE EN		0	This bit generates a long transport layer test pattern mode according to section 5.1.6.3 of the JESD204B specification. 0 = Test mode disabled 1 = Test mode enabled
3	0	W	0h	Must write 0
2	LANE ALIGN	R/W	0h	This bit inserts a lane alignment character (K28.3) for the receiver to align to the lane boundary per section 5.3.3.5 of the JESD204B specification. 0 = Normal operation 1 = Inserts lane alignment characters
1	FRAME ALIGN	R/W	0h	This bit inserts a frame alignment character (K28.7) for the receiver to align to the frame boundary per section 5.3.35 of the JESD204B specification. 0 = Normal operation 1 = Inserts frame alignment characters
0	TX LINK DIS	R/W	0h	This bit disables sending the initial link alignment (ILA) sequence when SYNC is deasserted. 0 = Normal operation 1 = ILA disabled

8.5.7.2 Register 002h (address = 002h), JESD Digital Page

Figure 88. Register 002h

7	6	5	4	3	2	1	0
SYNC REG	SYNC REG EN	0	0	12BIT MODE		JESD MODE0	
R/W-0h	R/W-0h	W-0h	W-0h	R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 49. Register 002h Field Descriptions

Bit	Field	Type	Reset	Description
7	SYNC REG	R/W	0h	SYNC control through SPI. 0 = Normal operation 1 = ADC output data is replaced with K28.5 characters
6	SYNC REG EN	R/W	0h	Enable bit for SYNC control through SPI. 0 = Normal operation 1 = SYNC Control through SPI enabled (ignores SYNCB input pins)
5-4	0	W	0h	Must write 0
3-2	12BIT MODE	R/W	0h	This bit enables the 12-bit output mode for more efficient data packing. 00 = Normal operation, 14-bit output 01, 10 = Unused 11 = High-efficient data packing enabled
1-0	JESD MODE0	R/W	0h	These bits select the configuration register to configure the correct LMFS frame assemblies for different decimation settings; see JESD frame assembly tables in the *JESD204B Frame Assembly* section. 00 = 0 01 = 1 10 = 2 11 = 3

8.5.7.3 Register 003h (address = 003h), JESD Digital Page

Figure 89. Register 003h

7	6	5	4	3	2	1	0
LINK LAYER TESTMODE			LINK LAY RPAT	LMFC MASK RES	JESD MODE1	JESD MODE2	RAMP 12BIT
R/W-0h			R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 50. Register 003h Field Descriptions

Bit	Field	Type	Reset	Description
7-5	LINK LAYER TESTMODE	R/W	0h	These bits generate a pattern according to section 5.3.3.8.2 of the JESD204B document. 000 = Normal ADC data 001 = D21.5 (high-frequency jitter pattern) 010 = K28.5 (mixed-frequency jitter pattern) 011 = Repeat initial lane alignment (generates a K28.5 character and repeats lane alignment sequences continuously) 100 = 12-octet RPAT jitter pattern
4	LINK LAY RPAT	R/W	0h	This bit changes the running disparity in a modified RPAT pattern test mode (only when link layer test mode = 100). 0 = Normal operation 1 = Changes disparity
3	LMFC MASK RES	R/W	0h	TBD
2	JESD MODE1	R/W	1h	These bits select the configuration register to configure the correct LMFS frame assemblies for different decimation settings; see JESD frame assembly tables in the *JESD204B Frame Assembly* section
1	JESD MODE2	R/W	0h	These bits select the configuration register to configure the correct LMFS frame assemblies for different decimation settings; see JESD frame assembly tables in the *JESD204B Frame Assembly* section
0	RAMP 12BIT	R/W	0h	This bit enables the RAMP test pattern for 12-bit mode only (LMFS = 82820). 0 = Normal data output 1 = Digital output is the RAMP pattern

8.5.7.4 Register 004h (address = 004h), JESD Digital Page

Figure 90. Register 004h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	REL ILA SEQ	
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 51. Register 004h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0
1-0	REL ILA SEQ	R/W	0h	These bits delay the generation of the lane alignment sequence by 0, 1, 2, or 3 multiframes after the code group synchronization. 00 = 0 multiframe delays 01 = 1 multiframe delay 10 = 2 multiframe delays 11 = 3 multiframe delays

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8.5.7.5 Register 006h (address = 006h), JESD Digital Page

Figure 91. Register 006h

7	6	5	4	3	2	1	0
SCRAMBLE EN	0	0	0	0	0	0	0
R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 52. Register 006h Field Descriptions

Bit	Field	Type	Reset	Description
7	SCRAMBLE EN	R/W	0h	Scramble enable bit in the JESD204B interface. 0 = Scrambling disabled 1 = Scrambling enabled
6-0	0	W	0h	Must write 0

8.5.7.6 Register 007h (address = 007h), JESD Digital Page

Figure 92. Register 007h

7	6	5	4	3	2	1	0
0	0	0	FRAMES PER MULTIFRAME (K)				
W-0h	W-0h	W-0h	R/W-0h				

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 53. Register 007h Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	W	0h	Must write 0
4-0	FRAMES PER MULTIFRAME (K)	R/W	0h	These bits set the number of multiframes. Actual K is the value in hex + 1 (that is, 0Fh is K = 16).

8.5.7.7 Register 016h (address = 016h), JESD Digital Page

Figure 93. Register 016h

7	6	5	4	3	2	1	0
0	40x MODE			0	0	0	0
W-0h	R/W-0h			W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 54. Register 016h Field Descriptions

Bit	Field	Type	Reset	Description
7	0	W	0h	Must write 0
6-4	40x MODE	R/W	0h	This register must be set for 40x mode operation. 000 = Register is set for 20x and 80x mode 111 = Register must be set for 40x mode
3-0	0	W	0h	Must write 0

8.5.7.8 Register 017h (address = 017h), JESD Digital Page

Figure 94. Register 017h

7	6	5	4	3	2	1	0
0	0	0	0	Lane0 POL	Lane1 POL	Lane2 POL	Lane3 POL
W-0h			R/W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 55. Register 017h Field Descriptions

Bit	Field	Type	Reset	Description
7		W	0h	Must write 0
6-4		R/W	0h	Must write 0
3-0	0	W	0h	Sets polarity of the individual JESD output lanes 0 = Polarity as given in the pinout (non-inverted) 1 = Inverts polarity (P/M)

8.5.7.9 Register 032h-035h (address = 032h-035h), JESD Digital Page

Figure 95. Register 032h

7	6	5	4	3	2	1	0
SEL EMP LANE 0						0	0
R/W-0h						W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 96. Register 033h

7	6	5	4	3	2	1	0
SEL EMP LANE 1						0	0
R/W-0h						W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 97. Register 034h

7	6	5	4	3	2	1	0
SEL EMP LANE 2						0	0
R/W-0h						W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 98. Register 035h

7	6	5	4	3	2	1	0
SEL EMP LANE 3						0	0
R/W-0h						W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 56. Register 032h-035h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	SEL EMP LANE	R/W	0h	These bits select the amount of de-emphasis for the JESD output transmitter. The de-emphasis value in dB is measured as the ratio between the peak value after the signal transition to the settled value of the voltage in one bit period. 0 = 0 dB 1 = –1 dB 3 = –2 dB 7 = –4.1 dB 15 = –6.2 dB 31 = –8.2 dB 63 = –11.5 dB
1-0	0	W	0h	Must write 0

8.5.7.10 Register 036h (address = 036h), JESD Digital Page

Figure 99. Register 036h

7	6	5	4	3	2	1	0
0	CMOS SYNCB	0	0	0	0	0	0
W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 57. Register 036h Field Descriptions

Bit	Field	Type	Reset	Description
7	0	W	0h	Must write 0
6	CMOS SYNCB	R/W	0h	This bit enables single-ended control of SYNCB using the GPIO4 pin (pin 63). The differential SYNCB input is ignored. 0 = Differential SYNCB input 1 = Single-ended SYNCB input using pin 63
5-0	0	W	0h	Must write 0

8.5.7.11 Register 037h (address = 037h), JESD Digital Page

Figure 100. Register 037h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	PLL MODE	
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 58. Register 037h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0
1-0	PLL MODE	R/W	0h	These bits select the PLL multiplication factor; see the JESD tables in the *JESD204B Frame Assembly* section for settings. 00 = 20x mode 01 = 16x mode 10 = 40x mode (the 40x MODE bit in register 16h must also be set) 11 = 80x mode

8.5.8 Decimation Filter Page

Direct Addressing, 16-Bit Address, 5000h for Channel A, 5800h for Channel B

8.5.8.1 Register 000h (address = 000h), Decimation Filter Page

Figure 101. Register 000h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DDC EN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 59. Register 000h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	DDC EN	R/W	0h	This bit enables the decimation filter and disables the bypass mode. 0 = Bypass mode (DDC disabled) 1 = Decimation filter enabled

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8.5.8.2 Register 001h (address = 001h), Decimation Filter Page

Figure 102. Register 001h

7	6	5	4	3	2	1	0
0	0	0	0	DECIM FACTOR			
W-0h	W-0h	W-0h	W-0h	R/W-0h			

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 60. Register 001h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0
3-0	DECIM FACTOR	R/W	0h	These bits configure the decimation filter setting. 0000 = Divide-by-4 complex 0001 = Divide-by-6 complex 0010 = Divide-by-8 complex 0011 = Divide-by-9 complex 0100 = Divide-by-10 complex 0101 = Divide-by-12 complex 0110 = Not used 0111 = Divide-by-16 complex 1000 = Divide-by-18 complex 1001 = Divide-by-20 complex 1010 = Divide-by-24 complex 1011 = Not used 1100 = Divide-by-32 complex

8.5.8.3 Register 002h (address = 2h), Decimation Filter Page

Figure 103. Register 002h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DUAL BAND EN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 61. Register 002h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	DUAL BAND EN	R/W	0h	This bit enables the dual-band DDC filter for the corresponding channel. 0 = Single-band DDC 1 = Dual-band DDC

8.5.8.4 Register 005h (address = 005h), Decimation Filter Page

Figure 104. Register 005h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	REAL OUT EN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 62. Register 005h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	REAL OUT EN	R/W	0h	This bit converts the complex output to real output at 2x the output rate. 0 = Complex output format 1 = Real output format

8.5.8.5 Register 006h (address = 006h), Decimation Filter Page

Figure 105. Register 006h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DDC MUX
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 63. Register 006h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	DDC MUX	R/W	0h	This bit connects the DDC to the alternate channel ADC to enable up to four DDCs with one ADC and completely turn off the other ADC channel. 0 = Normal operation 1 = DDC block takes input from the alternate ADC

8.5.8.6 Register 007h (address = 007h), Decimation Filter Page

Figure 106. Register 007h

7	6	5	4	3	2	1	0
DDC0 NCO1 LSB							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 64. Register 007h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DDC0 NCO1 LSB	R/W	0h	These bits are the LSB of the NCO frequency word for NCO1 of DDC0 (band 1). The LSB represents $f_S / (2^{16})$, where f_S is the ADC sampling frequency.

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8.5.8.7 Register 008h (address = 008h), Decimation Filter Page

Figure 107. Register 008h

7	6	5	4	3	2	1	0
DDC0 NCO1 MSB							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 65. Register 008h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DDC0 NCO1 MSB	R/W	0h	These bits are the MSB of the NCO frequency word for NCO1 of DDC0 (band 1). The LSB represents $f_S / (2^{16})$, where f_S is the ADC sampling frequency.

8.5.8.8 Register 009h (address = 009h), Decimation Filter Page

Figure 108. Register 009h

7	6	5	4	3	2	1	0
DDC0 NCO2 LSB							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 66. Register 009h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DDC0 NCO2 MSB	R/W	0h	These bits are the LSB of the NCO frequency word for NCO2 of DDC0 (band 1). The LSB represents $f_S / (2^{16})$, where f_S is the ADC sampling frequency.

8.5.8.9 Register 00Ah (address = 00Ah), Decimation Filter Page

Figure 109. Register 00Ah

7	6	5	4	3	2	1	0
DDC0 NCO2 MSB							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 67. Register 00Ah Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DDC0 NCO2 MSB	R/W	0h	These bits are the MSB of the NCO frequency word for NCO2 of DDC0 (band 1). The LSB represents $f_S / (2^{16})$, where f_S is the ADC sampling frequency.

8.5.8.10 Register 00Bh (address = 00Bh), Decimation Filter Page

Figure 110. Register 00Bh

7	6	5	4	3	2	1	0
DDC0 NCO3 LSB							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 68. Register 00Bh Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DDC0 NCO3 LSB	R/W	0h	These bits are the LSB of the NCO frequency word for NCO3 of DDC0 (band 1). The LSB represents $f_S / (2^{16})$, where f_S is the ADC sampling frequency.

8.5.8.11 Register 00Ch (address = 00Ch), Decimation Filter Page

Figure 111. Register 00Ch

7	6	5	4	3	2	1	0
DDC0 NCO3 MSB							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 69. Register 00Ch Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DDC0 NCO3 MSB	R/W	0h	These bits are the MSB of the NCO frequency word for NCO3 of DDC0 (band 1). The LSB represents $f_S / (2^{16})$, where f_S is the ADC sampling frequency.

8.5.8.12 Register 00Dh (address = 00Dh), Decimation Filter Page

Figure 112. Register 00Dh

7	6	5	4	3	2	1	0
DDC1 NCO4 LSB							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 70. Register 00Dh Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DDC1 NCO4 LSB	R/W	0h	These bits are the LSB of the NCO frequency word for NCO4 of DDC1 (band 2, only when dual-band mode is enabled). The LSB represents $f_S / (2^{16})$, where f_S is the ADC sampling frequency.

8.5.8.13 Register 00Eh (address = 00Eh), Decimation Filter Page

Figure 113. Register 00Eh

7	6	5	4	3	2	1	0
DDC1 NCO4 MSB							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 71. Register 00Eh Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DDC1 NCO4 MSB	R/W	0h	These bits are the MSB of the NCO frequency word for NCO4 of DDC1 (band 2, only when dual-band mode is enabled). The LSB represents f_S / (2^{16}), where f_S is the ADC sampling frequency.

8.5.8.14 Register 00Fh (address = 00Fh), Decimation Filter Page

Figure 114. Register 00Fh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	NCO SEL PIN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 72. Register 00Fh Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	NCO SEL PIN	R/W	0h	This bit enables NCO selection through the GPIO pins. 0 = NCO selection through SPI (see address 0h10) 1 = NCO selection through GPIO pins

8.5.8.15 Register 010h (address = 010h), Decimation Filter Page

Figure 115. Register 010h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	NCO SEL	
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 73. Register 010h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0
1-0	NCO SEL	R/W	0h	These bits enable NCO selection through register setting. 00 = NCO1 selected for band 1 01 = NCO2 selected for band 1 10 = NCO3 selected for band 1

8.5.8.16 Register 011h (address = 011h), Decimation Filter Page

Figure 116. Register 011h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LMFC RESET MODE	
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 74. Register 011h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0
1-0	LMFC RESET MODE	R/W	0h	These bits reset the configuration for all DDCs and NCOs. 00 = All DDCs and NCOs are reset with every LMFC RESET 01 = Reset with first LMFC RESET after DDC start. Afterwards, reset only when analog clock dividers are resynchronized. 10 = Reset with first LMFC RESET after DDC start. Afterwards, whenever analog clock dividers are resynchronized, use two LMFC resets. 11 = Do not use an LMFC reset at all. Reset the DDCs only when a DDC start is asserted and afterwards keep continuing. Deterministic latency is not ensured.

8.5.8.17 Register 014h (address = 014h), Decimation Filter Page

Figure 117. Register 014h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DDC0 6DB GAIN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 75. Register 014h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	DDC0 6DB GAIN	R/W	0h	This bit scales the output of DDC0 by 2 (6 dB) to compensate for real-to-complex conversion and image suppression. This scaling does not apply to the high-bandwidth filter path (divide-by-4 and -6); see register 1Fh. 0 = Normal operation 1 = 6-dB digital gain is added

8.5.8.18 Register 016h (address = 016h), Decimation Filter Page

Figure 118. Register 016h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DDC1 6DB GAIN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 76. Register 016h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	DDC1 6DB GAIN	R/W	0h	This bit scales the output of DDC0 by 2 (6 dB) to compensate for real-to-complex conversion and image suppression. This scaling does not apply to the high-bandwidth filter path (divide-by-4 and -6); see register 1Fh. 0 = Normal operation 1 = 6-dB digital gain is added

8.5.8.19 Register 01Eh (address = 01Eh), Decimation Filter Page

Figure 119. Register 01Eh

7	6	5	4	3	2	1	0
0	DDC DET LAT			0	0	0	0
W-0h	R/W-0h			W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 77. Register 01Eh Field Descriptions

Bit	Field	Type	Reset	Description
7	0	W	0h	Must write 0
6-4	DDC DET LAT	R/W	0h	These bits ensure deterministic latency depending on the decimation setting used; see Table 78.
3-0	0	W	0h	Must write 0

Table 78. DDC DET LAT Bit Settings

SETTING	COMPLEX DECIMATION SETTING
10h	Divide-by-24, -32 complex
20h	Divide-by-16, -18, -20 complex
40h	Divide-by-by 6, -12 complex
50h	Divide-by-4, -8, -9, -10 complex

8.5.8.20 Register 01Fh (address = 01Fh), Decimation Filter Page

Figure 120. Register 01Fh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	WBF 6DB GAIN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 79. Register 01Fh Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	WBF 6DB GAIN	R/W	0h	This bit scales the output of the wide bandwidth DDC filter by 2 (6 dB) to compensate for real-to-complex conversion and image suppression. This setting only applies to the high-bandwidth filter path (divide-by-4 and -6). 0 = Normal operation 1 = 6-dB digital gain is added

8.5.8.21 Register 033h-036h (address = 033h-036h), Decimation Filter Page

Figure 121. Register 033h

7	6	5	4	3	2	1	0
TEST PATTERN1[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Figure 122. Register 034h

7	6	5	4	3	2	1	0
TEST PATTERN1[15:8]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Figure 123. Register 035h

7	6	5	4	3	2	1	0
TEST PATTERN2[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Figure 124. Register 036h

7	6	5	4	3	2	1	0
TEST PATTERN2[15:8]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 80. Register 033h-036h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TEST PATTERN	R/W	0h	These bit set the custom test pattern in address 33h, 34h, 35h, or 36h.

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8.5.8.22 Register 037h (address = 037h), Decimation Filter Page

Figure 125. Register 037h

7	6	5	4	3	2	1	0
0	0	0	0	TEST PATTERN SEL			
W-0h	W-0h	W-0h	W-0h	R/W-0h			

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 81. Register 037h Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0	W	0h	Must write 0
3-0	TEST PATTERN SEL	R/W	0h	These bits select the test pattern output on the channel. 0000 = Normal operation using ADC output data 0001 = Outputs all 0s 0010 = Outputs all 1s 0011 = Outputs toggle pattern: output data are an alternating sequence of 10101010101010 and 01010101010101 0100 = Output digital ramp: output data increment by one LSB every clock cycle from code 0 to 16384 0110 = Single pattern: output data are custom pattern 1 (75h and 76h) 0111 = Double pattern: output data alternate between custom pattern 1 and custom pattern 2 1000 = Deskew pattern: output data are AAAAh 1001 = SYNC pattern: output data are FFFFh

8.5.8.23 Register 03Ah (address = 03Ah), Decimation Filter Page

Figure 126. Register 03Ah

7	6	5	4	3	2	1	0
0	0	0	0	0	0	TEST PAT RES	TP RES EN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 82. Register 03Ah Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0
1	TEST PAT RES	R/W	0h	Pulsing this bit resets the test pattern. The test pattern reset must be enabled first (bit D0). 0 = Normal operation 1 = Reset the test pattern
0	TP RES EN	R/W	0h	This bit enables the test pattern reset. 0 = Reset disabled 1 = Reset enabled

8.5.9 Power Detector Page

8.5.9.1 Register 000h (address = 000h), Power Detector Page

Figure 127. Register 000h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	PKDET EN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 83. Register 000h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	PKDET EN	R/W	0h	This bit enables the peak power and crossing detector. 0 = Power detector disabled 1 = Power detector enabled

8.5.9.2 Register 001h-002h (address = 001h-002h), Power Detector Page

Figure 128. Register 001h

7	6	5	4	3	2	1	0
BLKPKDET [7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Figure 129. Register 002h

7	6	5	4	3	2	1	0
BLKPKDET [15:8]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 84. Register 001h-002h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BLKPKDET	R/W	0h	This register specifies the block length in terms of number of samples (S`) used for peak power computation. Each sample S` is a peak of 8 actual ADC samples. This parameter is a 17-bit value directly in linear scale. In decimation mode, the block length must be a multiple of a divide-by-4 or -6 complex: length = 5 × decimation factor. The divide-by-8 to -32 complex: length = 10 × decimation factor.

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8.5.9.3 Register 003h (address = 003h), Power Detector Page

Figure 130. Register 003h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	BLKPKDET[16]
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 85. Register 003h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	BLKPKDET[16]	R/W	0h	This register specifies the block length in terms of number of samples (S`) used for peak power computation. Each sample S` is a peak of 8 actual ADC samples. This parameter is a 17-bit value directly in linear scale. In decimation mode, the block length must be a multiple of a divide-by-4 or -6 complex: length = 5 × decimation factor. The divide-by-8 to -32 complex: length = 10 × decimation factor.

8.5.9.4 Register 007h-00Ah (address = 007h-00Ah), Power Detector Page

Figure 131. Register 007h

7	6	5	4	3	2	1	0
BLKTHHH							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Figure 132. Register 008h

7	6	5	4	3	2	1	0
BLKTHHL							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Figure 133. Register 009h

7	6	5	4	3	2	1	0
BLKTHLH							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Figure 134. Register 00Ah

7	6	5	4	3	2	1	0
BLKTHLL							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 86. Register 007h-00Ah Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BLKTHHH BLKTHHL BLKTHLH BLKTHLL	R/W	0h	These registers set the four different thresholds for the hysteresis function threshold values from 0 to 256 (2TH), where 256 is equivalent to the peak amplitude. Example: BLKTHHH is set to –2 dBFS from peak: $10^{(-2 / 20)} \times 256$ = 203, then set 5407h, 5C07h = CBh.

8.5.9.5 Register 00Bh-00Ch (address = 00Bh-00Ch), Power Detector Page

Figure 135. Register 00Bh

7	6	5	4	3	2	1	0
DWELL[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Figure 136. Register 00Ch

7	6	5	4	3	2	1	0
DWELL[15:8]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 87. Register 00Bh-00Ch Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DWELL	R/W	0h	DWELL time counter. When the computed block peak crosses the upper thresholds BLKTHHH or BLKTHLH, the peak detector output flags are set. In order to be reset, the computed block peak must remain continuously lower than the lower threshold (BLKTHHL or BLKTHLL) for the period specified by the DWELL value. This threshold is 16 bits, is specified in terms of f_S / 8 clock cycles, and must be set to 0 for the crossing detector. Example: if f_S = 3 GSPS, f_S / 8 = 375 MHz, and DWELL = 0100h then the DWELL time = 2^9 / 375 MHz = 1.36 µs.

8.5.9.6 Register 00Dh (address = 00Dh), Power Detector Page

Figure 137. Register 00Dh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	FILT0LPSEL
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 88. Register 00Dh Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	FILT0LPSEL	R/W	0h	This bit selects either the block detector output or 2-bit output as the input to the IIR filter. 0 = Use the output of the high comparators (HH and HL) as the input of the IIR filter 1 = Combine the output of the high (HH and HL) and low (LH and LL) comparators to generate a 3-level input to the IIR filter (–1, 0, 1)

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8.5.9.7 Register 00Eh (address = 00Eh), Power Detector Page

Figure 138. Register 00Eh

7	6	5	4	3	2	1	0
0	0	0	0	TIMECONST			
W-0h	W-0h	W-0h	W-0h	R/W-0h			

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 89. Register 00Eh Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0
3-0	TIMECONST	R/W	0h	These bits set the crossing detector time period for N = 0 to 15 as $2^N \times f_S / 8$ clock cycles. The maximum time period is 32768 × $f_S / 8$ clock cycles (approximately 87 µs at 3 GSPS).

8.5.9.8 Register 00Fh, 010h-012h, and 016h-019h (address = 00Fh, 010h-012h, and 016h-019h), Power Detector Page

Figure 139. Register 00Fh

7	6	5	4	3	2	1	0
FIL0THH[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Figure 140. Register 010h

7	6	5	4	3	2	1	0
FIL0THH[15:8]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Figure 141. Register 011h

7	6	5	4	3	2	1	0
FIL0THL[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Figure 142. Register 012h

7	6	5	4	3	2	1	0
FIL0THL[15:8]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Figure 143. Register 016h

7	6	5	4	3	2	1	0
FIL1THH[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Figure 144. Register 017h

7	6	5	4	3	2	1	0
FIL1THH[15:8]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Figure 145. Register 018h

7	6	5	4	3	2	1	0
FIL1THL[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Figure 146. Register 019h

7	6	5	4	3	2	1	0
FIL1THL[15:8]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 90. Register 00Fh, 010h, 011h, 012h, 016h, 017h, 018h, and 019h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FIL0THH FIL0THL FIL1THH FIL1THL	R/W	0h	Comparison thresholds for the crossing detector counter. This threshold is 16 bits in 2.14 signed notation. A value of 1 (4000h) corresponds to 100% crossings, a value of 0.125 (0800h) corresponds to 12.5% crossings.

8.5.9.9 Register 013h-01Ah (address = 013h-01Ah), Power Detector Page

Figure 147. Register 013h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	IIR0 2BIT EN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 148. Register 01Ah

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	IIR1 2BIT EN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 91. Register 013h and 01Ah Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	IIR0 2BIT EN IIR1 2BIT EN	R/W	0h	This bit enables 2-bit output format of the IIR0 and IIR1 output comparators. 0 = Selects 1-bit output format 1 = Selects 2-bit output format

8.5.9.10 Register 01Dh-01Eh (address = 01Dh-01Eh), Power Detector Page

Figure 149. Register 01Dh

7	6	5	4	3	2	1	0
DWELLIIR[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Figure 150. Register 01Eh

7	6	5	4	3	2	1	0
DWELLIIR[15:8]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 92. Register 01Dh-01Eh Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DWELLIIR	R/W	0h	DWELL time counter for the IIR output comparators. When the IIR filter output crosses the upper thresholds FIL0THH or FIL1THH, the IIR peak detector output flags are set. In order to be reset, the output of the IIR filter must remain continuously lower than the lower threshold (FIL0THL or FIL1THL) for the period specified by the DWELLIIR value. This threshold is 16 bits and is specified in terms of f_S / 8 clock cycles. Example: if f_S = 3 GSPS, f_S / 8 = 375 MHz, and DWELLIIR = 0100h, then the DWELL time = 29 / 375 MHz = 1.36 µs.

8.5.9.11 Register 020h (address = 020h), Power Detector Page

Figure 151. Register 020h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	RMSDET EN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 93. Register 020h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	RMSDET EN	R/W	0h	This bit enables the RMS power detector. 0 = Power detector disabled 1 = Power detector enabled

8.5.9.12 Register 021h (address = 021h), Power Detector Page

Figure 152. Register 021h

7	6	5	4	3	2	1	0
0	0	0	PWRDETACCU				
W-0h	W-0h	W-0h	R/W-0h				

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 94. Register 021h Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	W	0h	Must write 0
4-0	PWRDETACCU	R/W	0h	These bits program the block length to be used for RMS power computation. The block length is defined in terms of f_S / 8 clocks and may be programmed as 2M, where M = 0 to 16.

8.5.9.13 Register 022h-025h (address = 022h-025h), Power Detector Page

Figure 153. Register 022h

7	6	5	4	3	2	1	0
PWRDETH[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Figure 154. Register 023h

7	6	5	4	3	2	1	0
PWRDETH[15:8]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Figure 155. Register 024h

7	6	5	4	3	2	1	0
PWRDETL[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Figure 156. Register 025h

7	6	5	4	3	2	1	0
PWRDETL[15:8]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 95. Register 022h-025h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWRDETH[15:0] PWRDETL[15:0]	R/W	0h	The computed average power is compared against these high and low thresholds. One LSB of the thresholds represents 1 / 2^{16}. Example: if PWRDETH is set to –14 dBFS from peak, $(10^{(-14 / 20)})^2 \times 2^{16} = 2609$, then set 5422h, 5423h, 5C22h, 5C23h = 0A31h.

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8.5.9.14 Register 027h (address = 027h), Power Detector Page

Figure 157. Register 027h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	RMS 2BIT EN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 96. Register 027h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	RMS 2BIT EN	R/W	0h	This bit enables 2-bit output format on the RMS output comparators. 0 = Selects 1-bit output format 1 = Selects 2-bit output format

8.5.9.15 Register 02Bh (address = 02Bh), Power Detector Page

Figure 158. Register 02Bh

7	6	5	4	3	2	1	0
0	0	0	RESET AGC	0	0	0	0
W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 97. Register 02Bh Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	W	0h	Must write 0
4	RESET AGC	R/W	0h	After configuration, the AGC module must be reset and then brought out of reset to start operation. 0 = Clear AGC reset 1 = Set AGC reset Example: set 542Bh to 10h and then to 00h.
3-0	0	W	0h	Must write 0

8.5.9.16 Register 032h-035h (address = 032h-035h), Power Detector Page

Figure 159. Register 032h

7	6	5	4	3	2	1	0
OUTSEL GPIO1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Figure 160. Register 033h

7	6	5	4	3	2	1	0
OUTSEL GPIO2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Figure 161. Register 034h

7	6	5	4	3	2	1	0
OUTSEL GPIO3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Figure 162. Register 035h

7	6	5	4	3	2	1	0
OUTSEL GPIO4							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 98. Register 032h-035h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUTSEL GPIO1 OUTSEL GPIO2 OUTSEL GPIO3 OUTSEL GPIO4	R/W	0h	These bits set the function or signal for each GPIO pin. 0 = IIR PK DET0[0] of channel A 1 = IIR PK DET0[1] of channel A (2-bit mode) 2 = IIR PK DET1[0] of channel A 3 = IIR PK DET1[1] of channel A (2-bit mode) 4 = BLKPKDETH of channel A 5 = BLKPKDETL of channel A 6 = PWR Det[0] of channel A 7 = PWR Det[1] of channel A (2-bit mode) 8 = FOVR of channel A 9-17 = Repeat outputs 0-8 but for channel B instead

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8.5.9.17 Register 037h (address = 037h), Power Detector Page

Figure 163. Register 037h

7	6	5	4	3	2	1	0
0	0	0	0	IODIR GPIO4	IODIR GPIO3	IODIR GPIO2	IODIR GPIO1
W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 99. Register 037h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0
3-0	IODIRGPIO[4:1]	R/W	0h	These bits select the output direction for the GPIO[4:1] pins. 0 = Input (for the NCO control) 1 = Output (for the AGC alarm function)

8.5.9.18 Register 038h (address = 038h), Power Detector Page

Figure 164. Register 038h

7	6	5	4	3	2	1	0
0	0	INSEL1		0	0	INSEL0	
W-0h	W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 100. Register 038h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0
5-4	INSEL1	R/W	0h	Selects which GPIO pin is used for the INSEL1 bit. 00 = GPIO4 01 = GPIO1 10 = GPIO3 11 = GPIO2 Table 101 lists the NCO selection, based on the bit settings of the INSEL pins.
3-2	0	W	0h	Must write 0
1-0	INSEL0	R/W	0h	Selects which GPIO pin is used for the INSEL0 bit. 00 = GPIO4 01 = GPIO1 10 = GPIO3 11 = GPIO2 Table 101 lists the NCO selection, based on the bit settings of the INSEL pins.

Table 101. INSEL Bit Settings

INSEL1	INSEL2	NCO SELECTED
0	0	NCO1
0	1	NCO2
1	0	NCO3
1	1	n/a

8.5.10 Initialization Registers Table

In the ADC32RF45 device, there are 56 registers located in the master page of the ADC page that must be initialized after power-up or reset with certain default values as listed in Table 102. The default value of these registers after reset is 00h.

Table 102. Address and Required Settings for the Initialization Registers

LOCATION: MASTER PAGE			LOCATION: MASTER PAGE			LOCATION: ADC PAGE		
SERIAL NUMBER	ADDRESS (Hex)	VALUE (Hex)	SERIAL NUMBER	ADDRESS (Hex)	VALUE (Hex)	SERIAL NUMBER	ADDRESS (Hex)	VALUE (Hex)
1	25	01h	20	53	60h	39	22	C0h
2	26	40h	21	59	02h	40	32	80h
3	27	80h	22	5B	08h	41	33	08h
4	29	40h	23	5C	07h	42	42	03h
5	2A	80h	24	62	E0h	43	43	03h
6	2C	40h	25	65	81h	44	45	58h
7	2D	80h	26	6B	04h	45	46	C4h
8	2F	40h	27	6C	08h	46	47	01h
9	34	01h	28	6E	80h	47	53	01h
10	3B	28h	29	6F	C0h	48	54	08h
11	3F	01h	30	70	C0h	49	5C	01h
12	40	80h	31	71	03h	50	64	05h
13	42	40h	32	76	A0h	51	72	84h
14	43	80h	33	77	0Ah	52	83	07h
15	45	40h	34	7D	41h	53	8C	80h
16	46	80h	35	81	18h	54	97	80h
17	48	40h	36	84	55h	55	F0	38h
18	49	80h	37	8A	41h	56	F1	BFh
19	4B	40h	38	8E	18h	—	—	—

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Start-Up Sequence

The steps detailed in Table 103 are recommended as the power-up sequence when the ADC32RF45 device is in bypass mode with a 12-bit output (LMFS = 82820).

Table 103. Initialization Sequence

STEP	SEQUENCE	DESCRIPTION	PAGE BEING PROGRAMMED	COMMENT
1	Supply all supply voltages.	For long term reliability and proper digital functionality, it is mandatory to bring up the 1.15V supplies before the 1.9 V supply.	—	
2	Provide the SYSREF signal.	—	Main digital page	—
3	Provide a reset.	—	—	—
	Pulse a hardware reset (low-to-high-to-low) on pin 48.	—	—	—
	Issue a software reset	Write address 0012h with 04h. Write address 0000h with 81h.	Master page	Issue a software reset
4	Program all analog trim registers on the ADC page.	Write address 0012h with 00h. Write address 0011h with FFh.	ADC page	Write the trim registers when the ADC page is selected. Do not write trim registers in 83h and 5Ch.
5	Program all analog trim registers on the master page.	Write address 0011h with 00h. Write address 0012h with 04h.	Master page	Write the trim registers when the master page is selected.
6	Program the final trim registers on the ADC page.	Write address 0012h with 00h.	ADC page	Write trim registers when the ADC page is selected.
		Write address 0011h with FFh.		
		Write address 0083h with 07h.		
		Write address 005Ch with 01h.		
7	Enable interleaving correction.	Write address 4003h with 00h.	Main digital page	Select channel A.
		Write address 4004h with 68h.		
		Write address 6044h with 20h.		Set LOOP EN1 for channel A.
		Write address 6068h with 40h.		Set LOOP EN2 for channel A.
		Write address 60A2h with 09h.		Enable and set the NQ zone.
		Write address 4003h with 01h.		Select channel B.
		Write address 6044h with 20h.		Set LOOP EN1 for channel B.
		Write address 6068h with 40h.		Set LOOP EN2 for channel B.
		Write address 60A2h with 09h.		Enable and set the NQ zone.
8	Issue software reset	Write address 6000h with 01h.	Main digital page	Issue and clear the reset for channel A.
		Write address 6000h with 00h.		
		Write address 4003h with 01h.		Set the digital page to 6801h for channel B.
		Write address 6000h with 01h.		Issue and clear the reset for channel B.
		Write address 6000h with 00h.		

Table 103. Initialization Sequence (continued)

STEP	SEQUENCE	DESCRIPTION	PAGE BEING PROGRAMMED	COMMENT
9	Set registers for digital bank	Write address 4003h with 00h.	JESD digital page	Select JESD digital page.
		Write address 4004h with 69h.		
		Write address 6002h with 0Fh.		Enable the 12-bit mode output, channel A.
		Write address 6003h with 00h.		Set JESD MODE1/2 = 0, channel A.
		Write address 6037h with 01h.		Set PLL to 16x, channel A.
		Write address 6001h with 80h.		Set CTRL K for channel A.
		Write address 6006h with 0Fh.		Set K = 16, channel A.
		Write address 7002h with 0Fh.		Enable the 12-bit mode output, channel B.
		Write address 7003h with 00h.		Set JESD MODE1, 2 = 0, channel B.
		Write address 7037h with 01h.		Set PLL to 16x, channel B.
		Write address 7001h with 80h.		Set CTRL K for channel B.
		Write address 7006h with 0Fh.		Set K = 16, channel B.
10	Pulse the SYNCB pin from low to high to transmit data from K28.5 sync mode.	—	—	

9.1.2 Hardware Reset

Timing information for the hardware reset is shown in Figure 165 and Table 104.

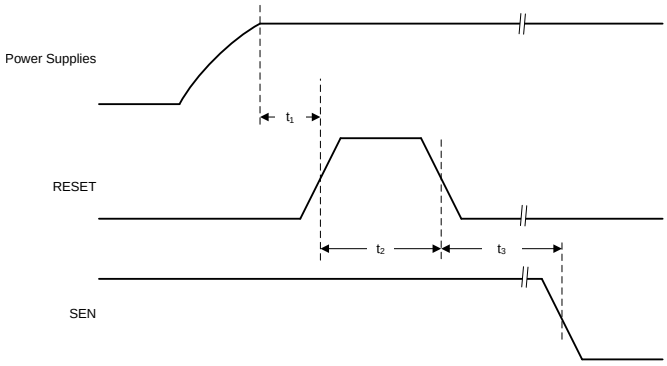

Figure 165. Hardware Reset Timing Diagram

Table 104. Hardware Reset Timing Information

		MIN	TYP	MAX	UNIT
t_1	Power-on delay from power-up to active high RESET pulse	1			ms
t_2	Reset pulse duration: active high RESET pulse duration	1			µs
t_3	Register write delay from RESET disable to SEN active	100			ns

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9.1.3 SNR and Clock Jitter

The signal-to-noise ratio (SNR) of the ADC is limited by three different factors: quantization noise, thermal noise, and jitter, as shown in Equation 5. The quantization noise is typically not noticeable in pipeline converters and is 84 dB for a 14-bit ADC. The thermal noise limits the SNR at low input frequencies and the clock jitter sets the SNR for higher input frequencies.

$$SNRADC\left[dBc\right] = -20\log\sqrt{\left(10^{-\frac{SNR_{Quantization\ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Thermal\ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Jitter}}{20}}\right)^2} \quad (5)$$

The SNR limitation resulting from sample clock jitter may be calculated by Equation 6:

$$SNR_{Jitter}\left[dBc\right] = -20\log\left(2\pi \times f_{IN} \times t_{Jitter}\right) \quad (6)$$

The total clock jitter (T_{Jitter}) has two components: the internal aperture jitter (70 f_S) is set by the noise of the clock input buffer and the external clock jitter. T_{Jitter} may be calculated by Equation 7:

$$t_{Jitter} = \sqrt{\left(t_{Jitter,\ Ext\_Clock\_Input}\right)^2 + \left(t_{Aperture\_ADC}\right)^2} \quad (7)$$

External clock jitter may be minimized by using high-quality clock sources and jitter cleaners as well as band-pass filters at the clock input. A faster clock slew rate also improves the ADC aperture jitter.

The ADC32RF45 device has a thermal noise of approximately 63 dBFS and an internal aperture jitter of 70 f_S. The SNR, depending on the amount of external jitter for different input frequencies, is shown in Figure 166.

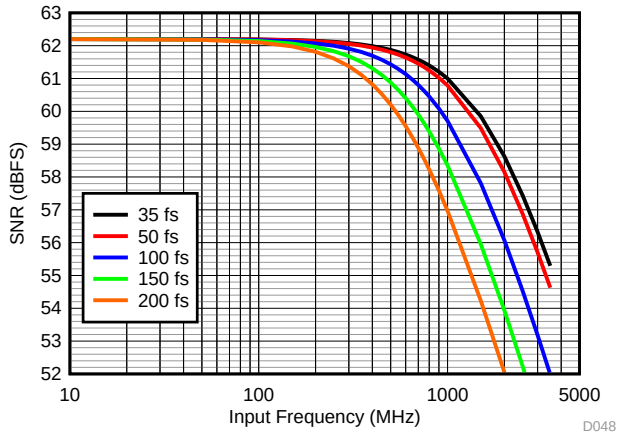

Figure 166. ADC SNR vs Input Frequency and External Clock Jitter

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9.1.3.1 External Clock Phase Noise Consideration

External clock jitter may be calculated by integrating the phase noise of the clock source out to approximately two times of the ADC sampling rate ($2 \times f_S$), as shown in Figure 167. In order to maximize the ADC SNR, an external band-pass filter is recommended to be used on the clock input. This filter reduces the jitter contribution from the broadband clock phase noise floor by effectively reducing the integration bandwidth to the pass band of the band-pass filter. This method is suitable when estimating the overall ADC SNR resulting from clock jitter at a certain input frequency.

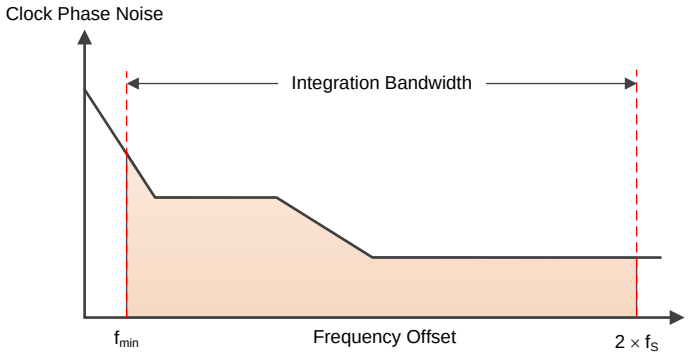


Figure 167. Integration Bandwidth for Extracting Jitter from Clock Phase Noise

However, when estimating the affect of a nearby blocker (such as a strong in-band interferer) to the sensitivity, the phase noise information may be used directly to estimate the noise budget contribution at a certain offset frequency, as shown in Figure 168.

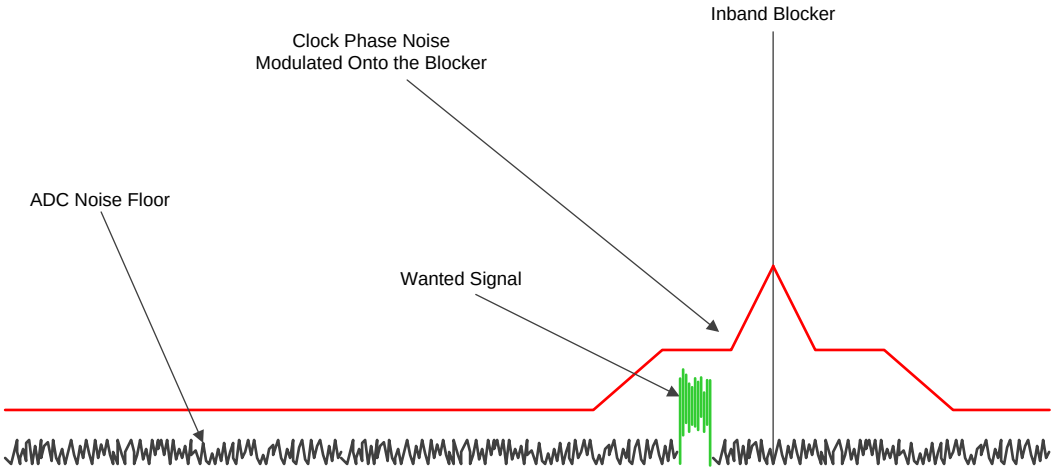


Figure 168. Small Wanted Signal in Presence of Interferer

At the sampling instant, the phase noise profile of the clock source convolves with the input signal (for example, the small wanted signal and the strong interferer merge together). If the power of the clock phase noise in the signal band of interest is too large, the wanted signal cannot not be recovered.

The resulting equivalent phase noise at the ADC input is also dependent on the sampling rate of the ADC and frequency of the input signal. The ADC sampling rate scales the clock phase noise, as shown in Equation 8.

$$ADC_{NSD}\left(dBc / Hz\right) = PN_{CLK}\left(dBc / Hz\right) - 20 \times \log\left(\frac{f_S}{f_{IN}}\right) \quad (8)$$

Using this information, the noise contribution resulting from the phase noise profile of the ADC sampling clock may be calculated.

9.2 Typical Application

The ADC32RF45 device is designed for wideband receiver applications demanding high dynamic range over a large input frequency range. A typical schematic for an ac-coupled receiver is shown in Figure 169.

Decoupling capacitors with low ESL are recommended to be placed as close as possible at the pins indicated in Figure 169. Additional capacitors may be placed on the remaining power pins.

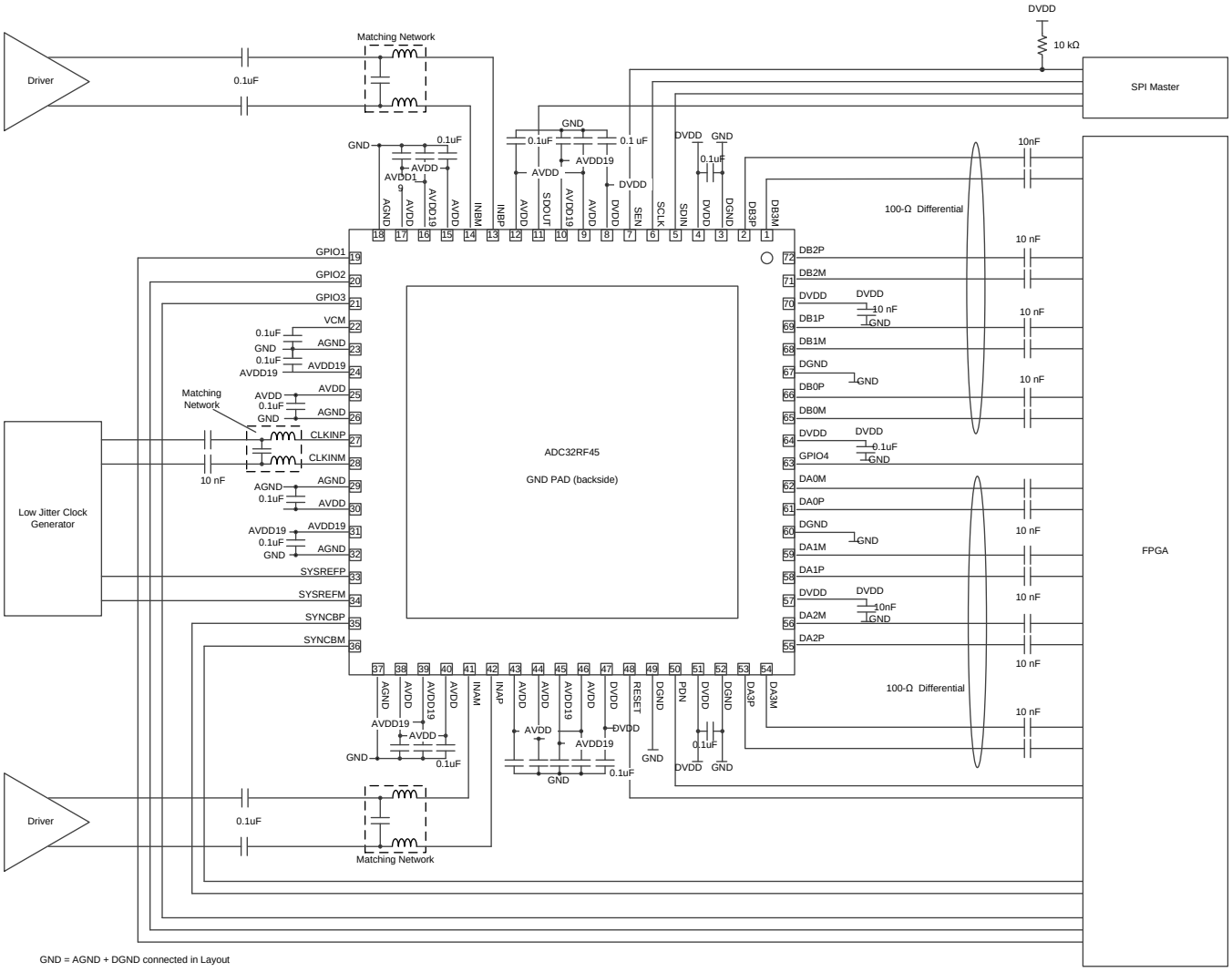


Figure 169. Typical Application Implementation Diagram

Typical Application (continued)

9.2.1 Design Requirements

9.2.1.1 Transformer-Coupled Circuits

Typical applications involving transformer-coupled circuits are discussed in this section. To ensure good amplitude and phase balance at the analog inputs, transformers (such as TC1-1-13 and TC1-1-43) may be used from the dc to 600-MHz range and from the 600-MHz to 4-GHz range of input frequencies, respectively. When designing the driving circuits, the ADC input impedance (or $S_{DD}11$) must be considered.

By using the simple drive circuit of Figure 170, uniform performance may be obtained over a wide frequency range. The buffers present at the analog inputs of the device help isolate the external drive source from the switching currents of the sampling circuit.

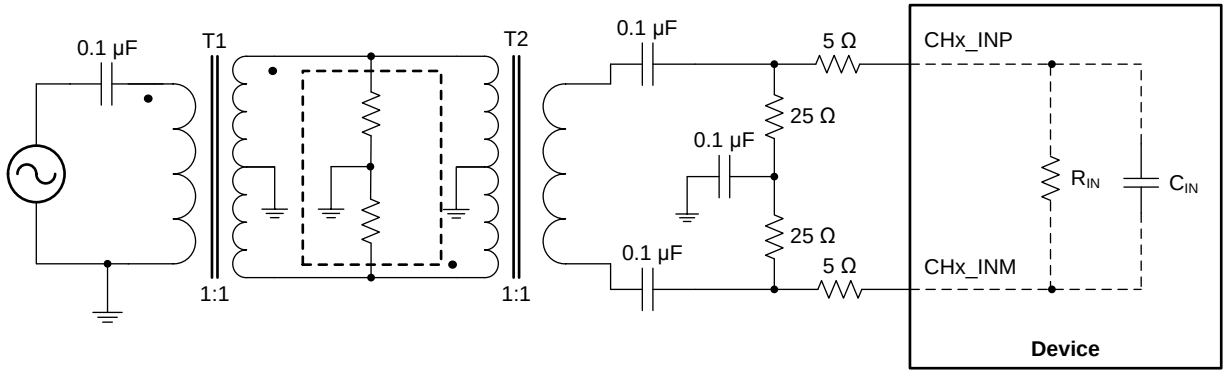


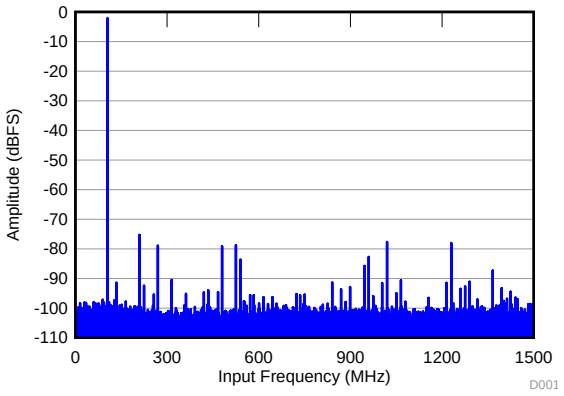
Figure 170. Input Drive Circuit

9.2.2 Detailed Design Procedure

For optimum performance, the analog inputs must be driven differentially. This architecture improves common-mode noise immunity and even-order harmonic rejection. A small resistor (5 Ω to 10 Ω) in series with each input pin is recommended to damp out ringing caused by package parasitics, as shown in Figure 170.

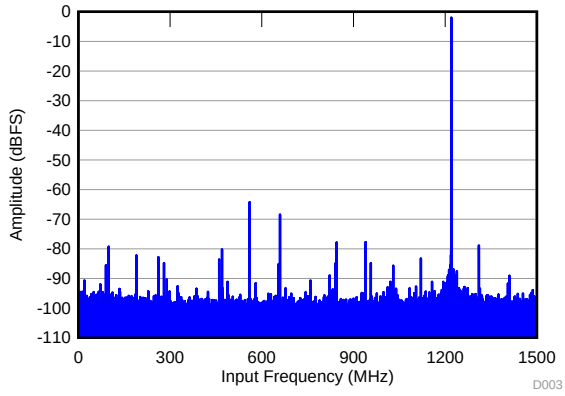
9.2.3 Application Curves

Figure 171 and Figure 172 show the typical performance at 100 MHz and 1780 MHz, respectively.



SNR = 61.8 dBFS, SINAD = 61.2 dBFS,
HD2 = 71 dBc, HD3 = 75 dBc, SFDR = 71 dBc,
THD = 68 dBc, IL spur = 77 dBc, worst spur = 73 dBc

Figure 171. FFT for 100-MHz Input Frequency



SNR = 57.9 dBFS, SINAD = 57.1 dBFS,
HD2 = 63 dBc, HD3 = 66 dBc, SFDR = 63 dBc,
THD = 60 dBc, IL spur = 79 dBc, worst spur = 77 dBc

Figure 172. FFT for 1780-MHz Input Frequency

PRODUCT PREVIEW

10 Power Supply Recommendations

The device requires a 1.15-V nominal supply for DVDD, a 1.15-V nominal supply for AVDD, and a 1.9-V nominal supply for AVDD19. There is no specific sequence for power-supply requirements during device power-up. AVDD, DVDD, and AVDD19 may power-up in any order.

11 Layout

11.1 Layout Guidelines

The device evaluation module (EVM) layout may be used as a reference layout to obtain the best performance. A layout diagram of the EVM top layer is provided in Figure 173. The (*ADC32RF45EVM User's Guide*), provides a complete layout of the EVM. Some important points to remember during board layout are:

- Analog inputs are located on opposite sides of the device pinout to ensure minimum crosstalk on the package level. To minimize crosstalk onboard, the analog inputs must exit the pinout in opposite directions, as shown in the reference layout of Figure 173 as much as possible.
- In the device pinout, the sampling clock is located on a side perpendicular to the analog inputs in order to minimize coupling between them. This configuration is also maintained on the reference layout of Figure 173 as much as possible.
- Keep digital outputs away from the analog inputs. When these digital outputs exit the pinout, the digital output traces must not be kept parallel to the analog input traces because this configuration may result in coupling from the digital outputs to the analog inputs and degrade performance. All digital output traces to the receiver [such as a field-programmable gate arrays (FPGAs) or application-specific integrated circuits (ASICs)] must be matched in length to avoid skew among outputs.
- At each power-supply pin (AVDD, DVDD, or AVDDD3V), keep a 0.1-µF decoupling capacitor close to the device. A separate decoupling capacitor group consisting of a parallel combination of 10-µF, 1-µF, and 0.1-µF capacitors may be kept close to the supply source.

11.2 Layout Example

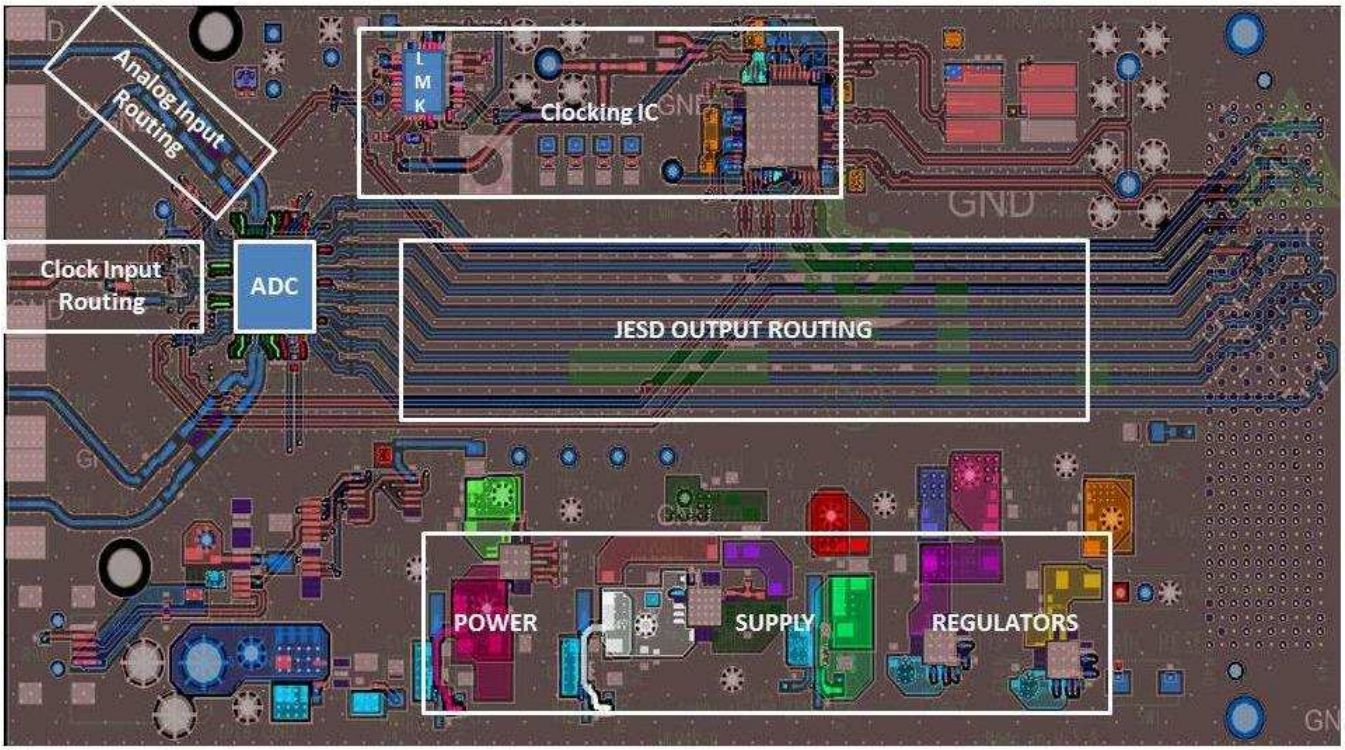


Figure 173. ADC32RF45 Device EVM Layout

PRODUCT PREVIEW

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

ADC32RF4x EVM User's Guide

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC32RF45IRMP	PREVIEW	VQFN	RMP	72	168	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ32RF45	
ADC32RF45IRMPT	PREVIEW	VQFN	RMP	72	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ32RF45	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

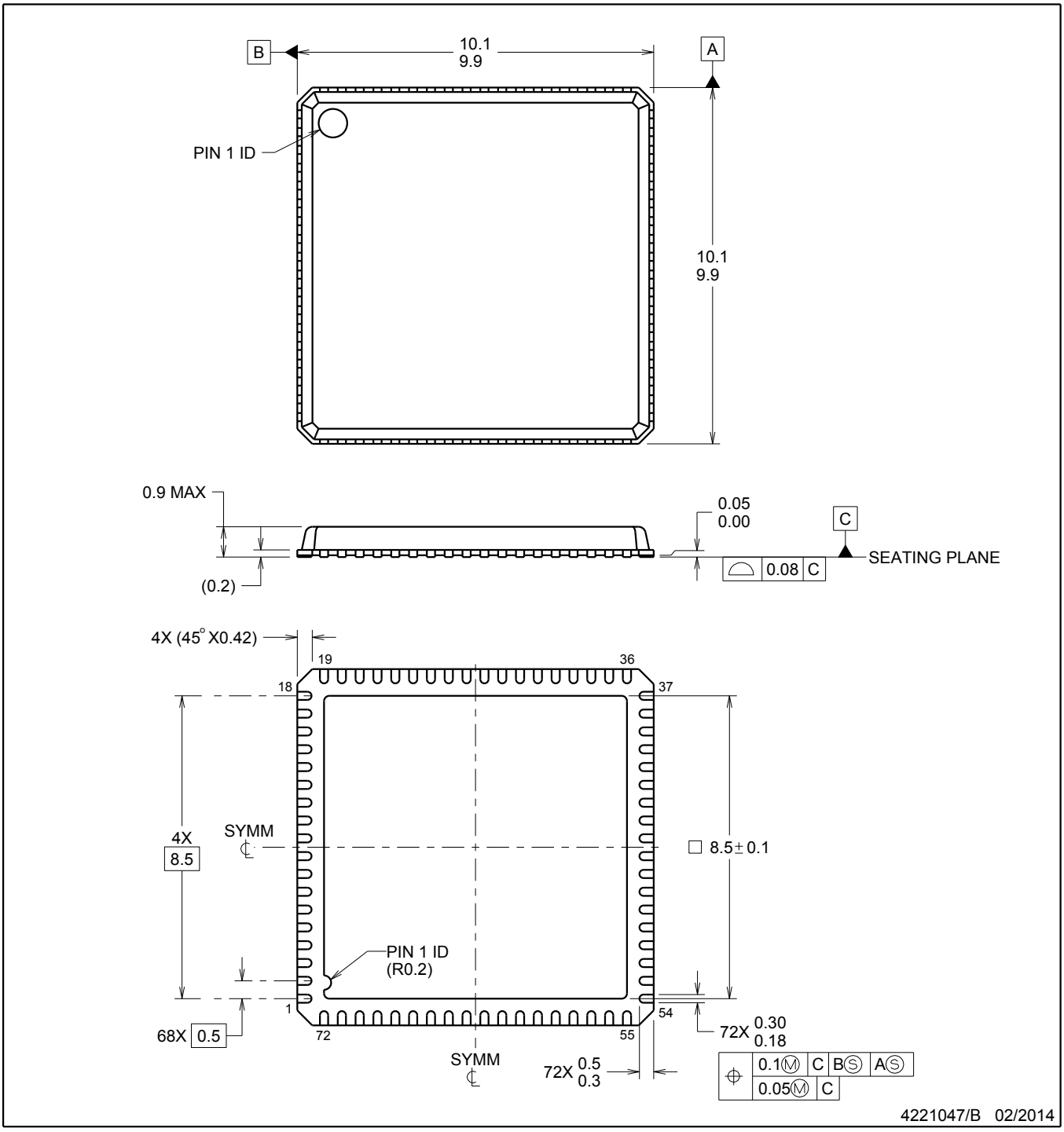
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

RMP0072A

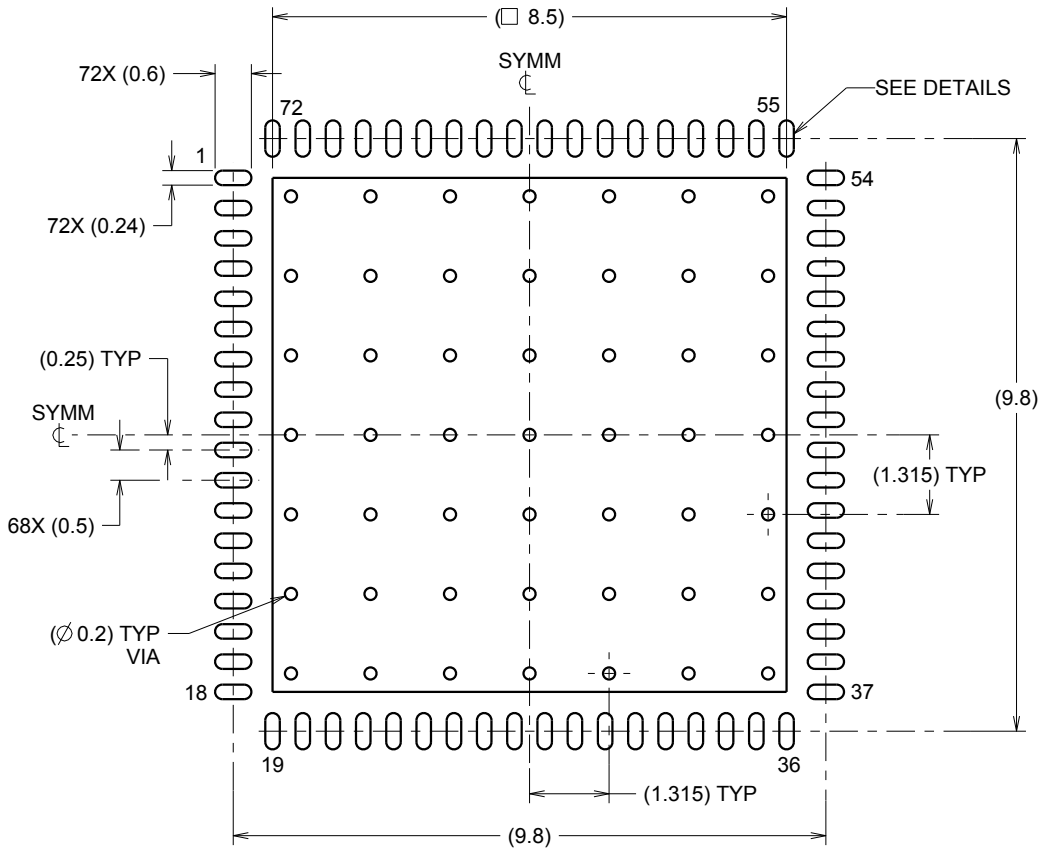
VQFN - 0.9 mm max height

VQFN

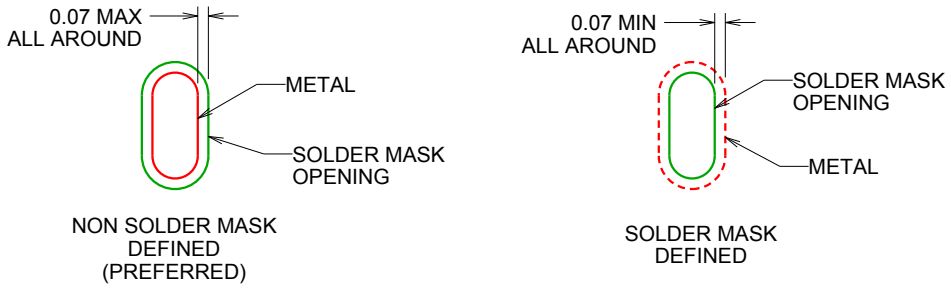


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:8X

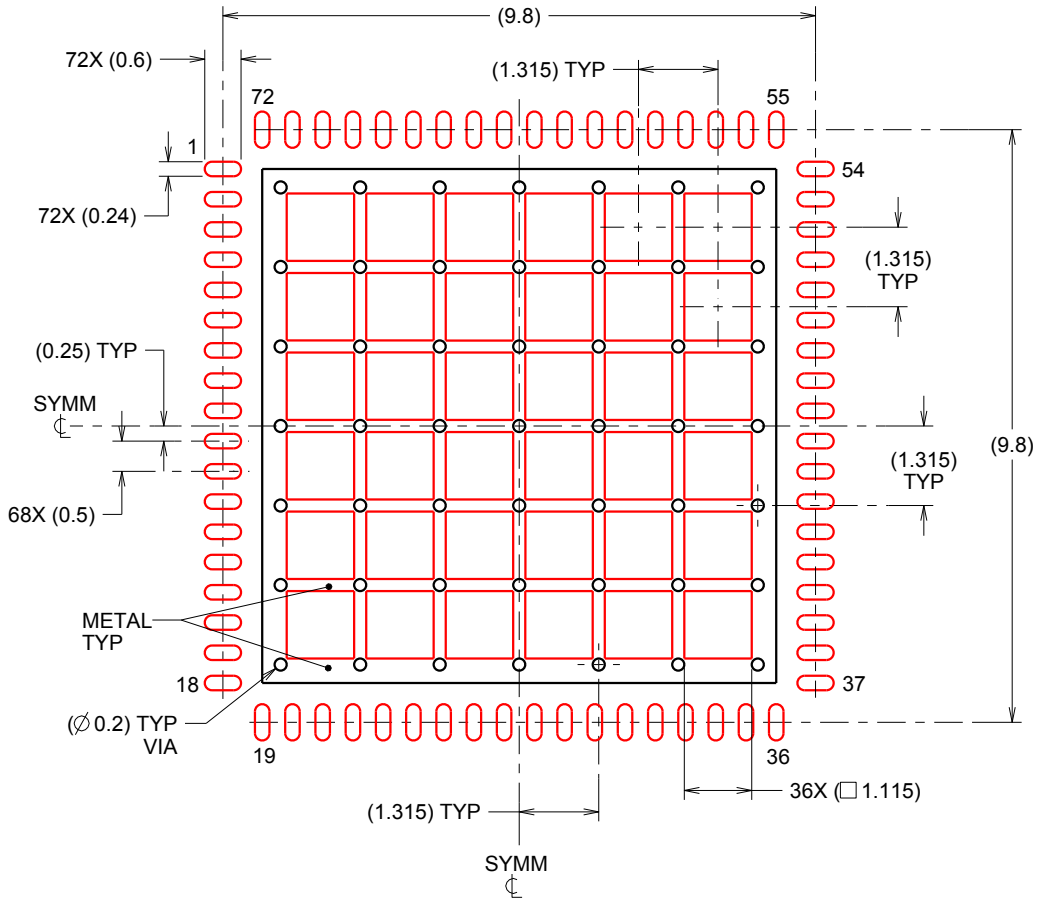


SOLDER MASK DETAILS

4221047/B 02/2014

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
62% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

4221047/B 02/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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